AX58101/AX58102
EtherCAT SubDevice Controller

Features

Document No: AX58101(2)/V1.01/28/01/26

- **EtherCAT SubDevice Controller (ESC) with 2 Integrated Fast Ethernet PHYs**
  - 2 Integrated Fast Ethernet PHYs and 3rd & 4th Ethernet MII Ports for Flexible EtherCAT Network Configuration
  - Supports ESC Port 0 and Port 2 interface Swapping
  - 8 Fieldbus Memory Management Units (FMMUs)
  - 8 Sync Managers
  - 8K bytes RAM
  - 64-bit distributed clock
- **Integrated Fast Ethernet PHYs**
  - Compliant with IEEE 802.3/802.3u 100BASE-TX/100BASE-FX
  - PHY loopback mode
  - Supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Automatic polarity detection and correction
- **Support up to 32(AX58101)/64(AX58102) DIO/GPIOs**
  - Individually configurable IOs, directly mapped to FMMU
- **SPI Slave Interface**
  - Supports Mode 3 timing modes
  - Supports MSB first transfer fashion
- **Local Bus Interface**
  - Supports 8-bit or 16-bit data bus width
  - Supports Asynchronous Local Bus
  - Supports BHE with 16-bit data bus width
  - Supports Asynchronous Multiplexed Address/Data (A/D merging) Bus
- **3-channel PWM Controller**
  - Adjustable frequency, phase align and BBM (Break Before Make) for all channels
  - Adjustable duty cycle, phase shift, and signal polarity per channel
- **Step & Direction Controller**
  - Adjustable step pulse width, polarity and the delay time for direction change
- **Incremental and Hall Encoder Interface**
  - Support single ended ABZ with configurable counting constant, polarity and Multiple Z-signal functions support
  - Supports clockwise/counter clockwise (CW/CCW) and direction-count (DIR/CLK) Inputs
  - Supports Hall sensor
- **Emergency Stop Input**
- **Configurable Watchdog for Outputs and Inputs Monitoring**
- **IRQ Event Output**
  - Interrupts for EtherCAT related events
  - Interrupts for Application related events
  - Interrupts for Watchdog Timeout
- **SPI Master Interface**
  - Programmable SPI clock frequency up to 50MHz
  - Supports 4 timing modes
  - Supports MSB/LSB first transfer fashion
  - Supports up to 8 SPI devices selection
  - Supports up to 8 channels, each channel with 8 bytes read/write buffer
  - Supports ADC Data Ready and DAC Data Loaded indication
  - Supports periodic data acquisition
  - Supports late sample for high latency device
  - Supports external interrupt input
- **Supports I^2C Master Interface**
- **Integrates On-chip Power-on Reset Circuit**
- **80-pin(AX58101)/128-pin(AX58102) LQFP RoHS Compliant Package**
- **Operating Temperature Range: -40 to +105°C**

Target Applications

- Motion/Motor Control
- Digital I/O Control
- Robotics
- Sensors Data Acquisition
- EtherCAT to IO-Link Gateway
- EtherCAT Junction Module
- Communication Module
- Operator HMI Interfaces

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Typical Applications Diagram

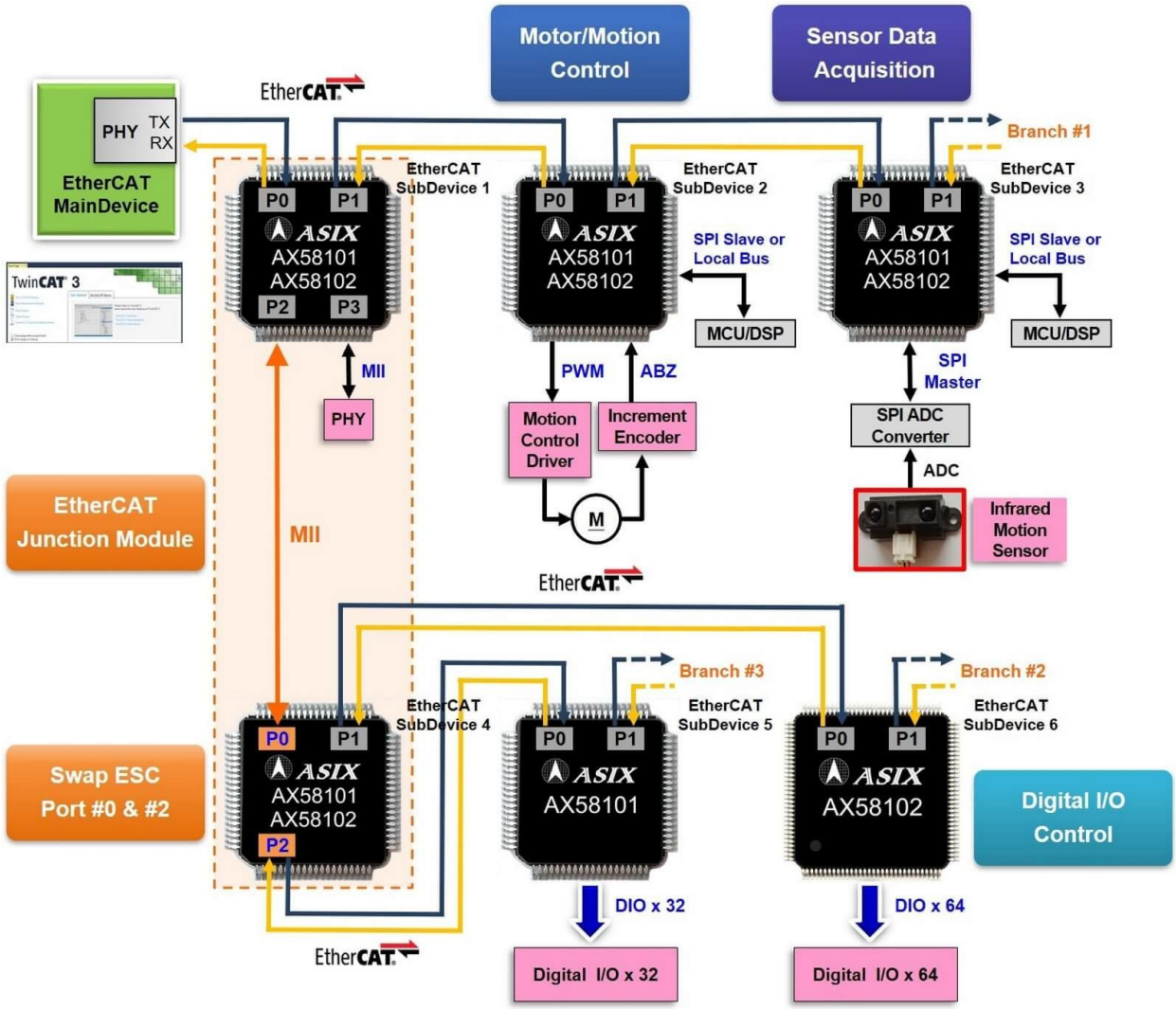

Figure 0-1: AX58101(2) Typical Applications Diagram

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1 Introduction

1.1 General Description

The AX58101(2) is an EtherCAT SubDevice Controller (ESC), licensed from Beckhoff Automation, with two integrated Fast Ethernet PHYs which support 100Mbps full-duplex operation and HP Auto-MDIX. The AX58101(2) supports the CANopen over EtherCAT (CoE), File Access over EtherCAT (FoE), Vendor Specific-protocol over EtherCAT (VoE), etc. Standard EtherCAT protocols provide a cost-effective solution for industrial automation applications, such as motion/motor/digital I/O control, Digital to Analog (DAC)/Analog to Digital (ADC) converters control, sensors data acquisition, and robotics, to be applied in industrial fieldbus.

The AX58101(2) provides either a three-channel PWM controller or a Step/Direction controller, and also provides an Increment/Hall encoder interface for closed-loop motor control, a SPI master controller for DAC/ADC converter control and sensors data acquisition, 32 DIOs for industrial I/O control and an I/O watchdog for functional safety.

The AX58101(2) provides two Process Data Interfaces (PDI), SPI slave and Local Bus, which support the connection with most popular MCU and DSP on those non-EtherCAT fieldbus applications. The AX58101(2) also provides two memory spaces, ESC and Function, users can decide which to access by using chip select to access the functions (PWM, SPI master etc.). The AX58101(2) reports the ESC and Functions interrupt events to interrupt status registers and supports level or edge interrupt trigger mode to inform external MCU/DSP to manage these ESC and Functions interrupt events. AX58101(2) supports a configurable individual function SPI slave interface to enhance SPI slave bandwidth.

The AX58101(2), in 80(128)-pin LQFP with EPAD, supports the RoHS compliant package and industrial grade operating temperature, which range from -40 to 105°C.

1.2 Block Diagram

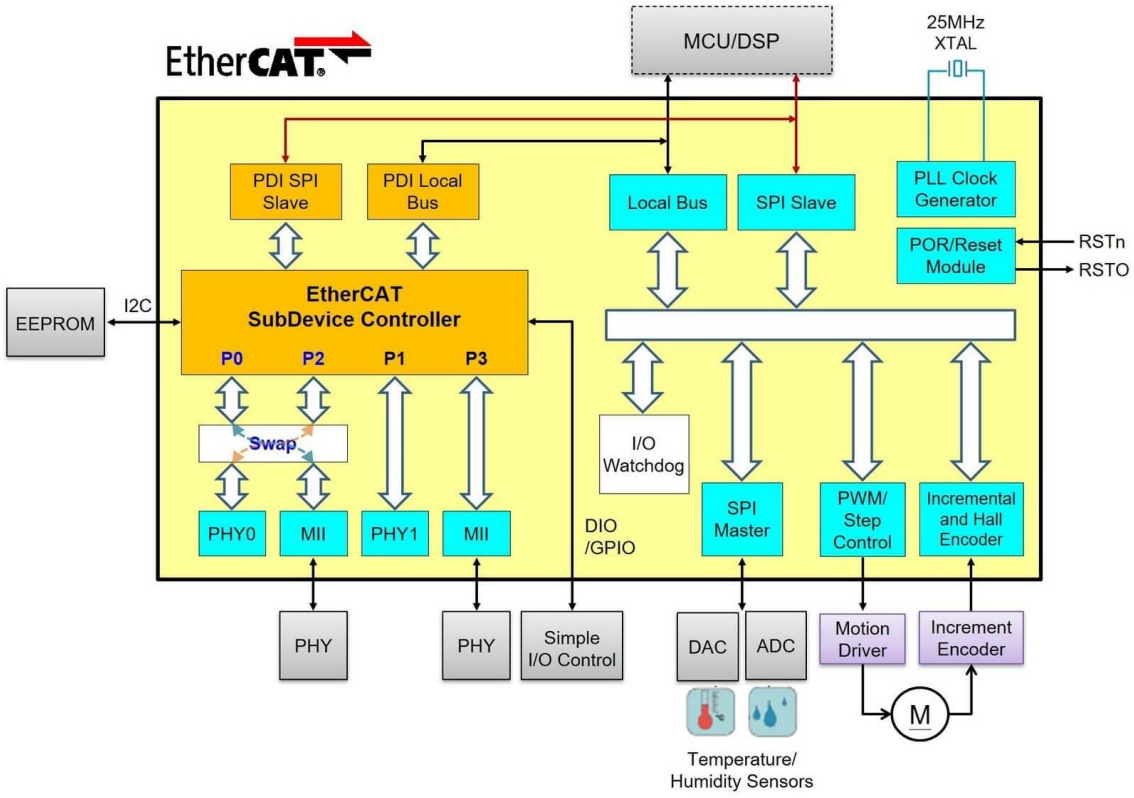

Figure 1-1: AX58101(2) Block Diagram

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1.3 Pinout Diagram

1.3.1 AX58101 is housed in an 80-pin E-PAD LQFP package

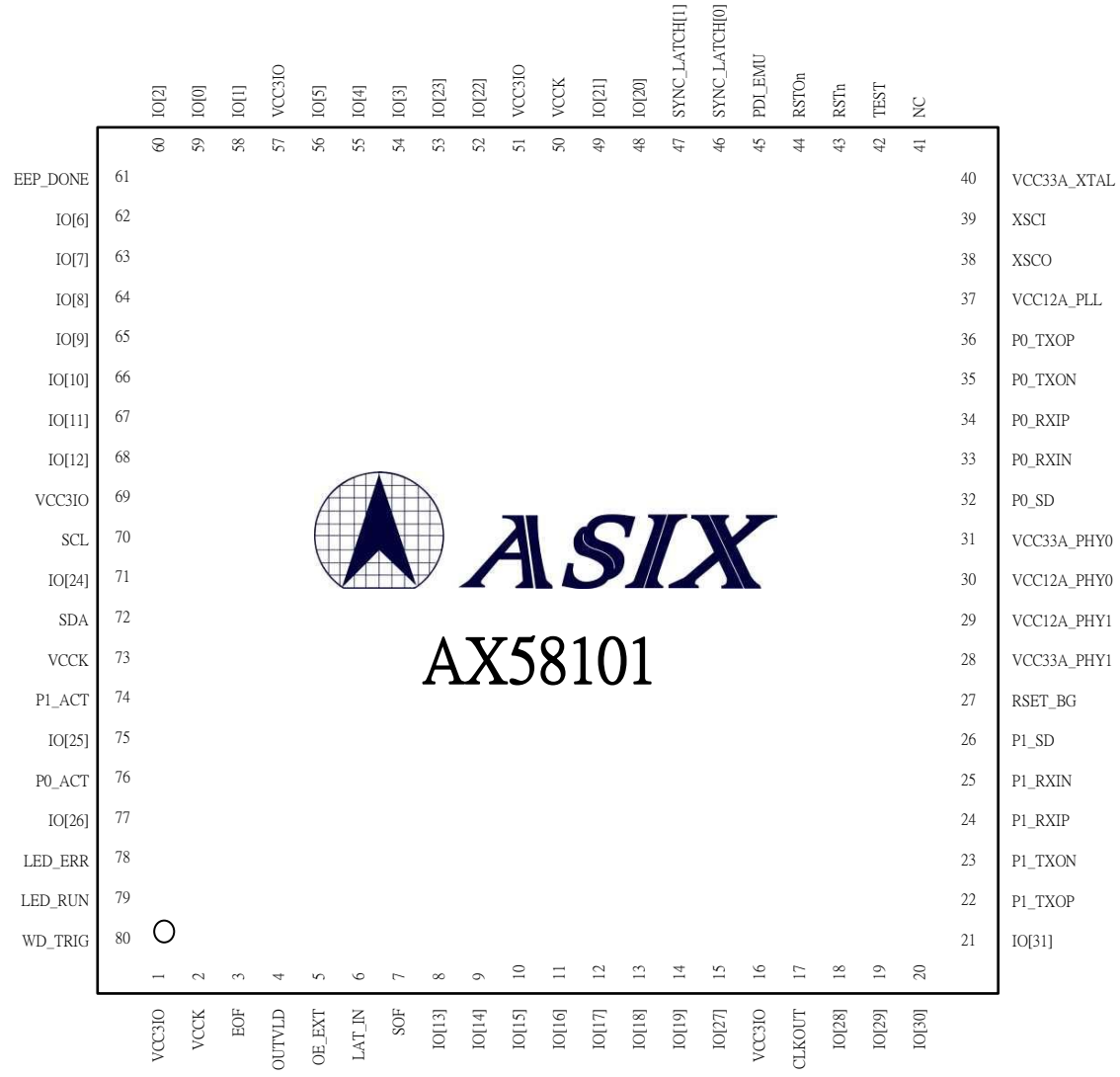

Figure 1-2: AX58101 Pinout Diagram

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1.3.2 AX58102 is housed in a 128-pin E-PAD LQFP package

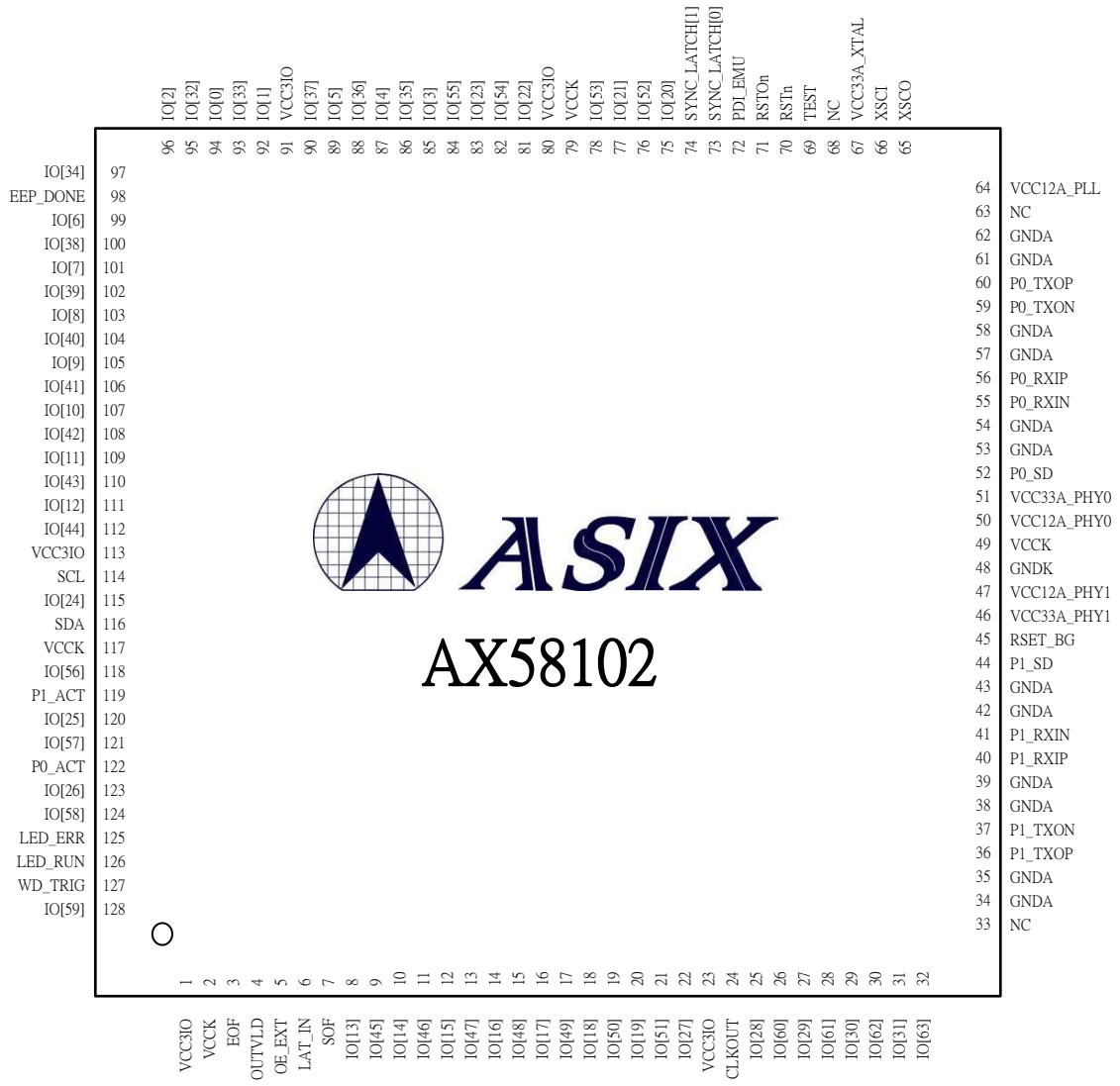

Figure 1-3: AX58102 Pinout Diagram

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1.4 Signal Description

Following abbreviations are used in "Type" column of below pin description tables. Note that some I/O pins with multiple signal definitions on the same pin may have different attributes in "Type" column for different signal definition.

AB	Analog Bi-directional I/O	**PU**	Internal Pull-Up (75K)
AI	Analog Input	**PD**	Internal Pull-Down (75K)
AO	Analog Output	**P**	Power/Ground pin
B5	Bi-directional I/O, 3.3V with 5V tolerant	**S**	Schmitt Trigger
I5	Input, 3.3V with 5V tolerant	**T**	Tri-state
O5	Output, 3.3V with 5V tolerant	**4m**	4mA driving strength
I3	Input, 3.3V	**8m**	8mA driving strength
O3	Output, 3.3V		

For example, pin 6 in AX58101(2) package can be LAT_IN, MISO or LRDY. If LAT_IN is selected, its Type is I5; if MISO or LRDY is selected, its Type is O5 or O5/T. In other words, the T (tri-state) only takes effect in LRDY signal mode while LAT_IN and MISO signal mode don't. Users should refer to the table specific to the desired function for exact pin type definition.

The multi-function pin settings are configured by the I^2C Hardware Configuration EEPROM (HWCFGEE). Please refer to Section 3.2 for details.

1.4.1 General

Table 1-1: Common Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP 128	
TEST	I5/PD/S	42	69	Test mode enable For normal operation, please always tie to logic low or NC.
RSTn	I5/PU/S	43	70	Reset Input, active low RST_N is the hardware reset input used to reset this chip. This input is AND with internal Power-On-Reset (POR) circuit, which generates the main system reset for this chip.
RSTO\ RSTO_POL	O5/8m	44	71	Reset Output This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the RSTO polarity, please refer to Section 3.1.
XSCI	AI	39	66	Crystal 25MHz Input, 3.3V
XSCO	AB	38	65	Crystal 25MHz Output
SCL	O5/T/4m/S	70	114	I^2C Serial Clock line for I^2C master controller SCL is a tri-stateable output, which requires an external pull-up resistor.
SDA	B5/T/4m/S	72	116	I^2C Serial Data line for I^2C master controller. SDA is a tri-stateable output, which requires an external pull-up resistor.
PDI_EMU	I5	45	72	PDI Emulation enable
EEP_DONE	O5/8m	61	98	This pin asserted high indicates that the EEPROM is successfully loaded (Checksum matched) and the PDI can be used.
LED_RUN\ EEP_SIZE	B5/4m	79	126	LED_RUN is input direction during chip reset stage used to bootstrap the mode setting to decide the EEPROM size configuration, please refer to Section 3.1.
LED_ERR\ 3PORT_MODE	B5/4m	78	125	LED_ERR is input direction during chip reset stage used to bootstrap the mode setting to decide the Port 2 MII enable

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				configuration, please refer to Section 3.1.
SYNC_LATCH[0]	B5/8m	46	73	Distributed Clocks SyncSignal output or LatchSignal input 0
SYNC_LATCH[1]	B5/8m	47	74	Distributed Clocks SyncSignal output or LatchSignal input 1 SYNC_LATCH[1] is input direction during chip reset stage used to bootstrap the mode setting to decide the SPI late samp enable configuration when none EEPROM mode, please refer to Section 3.1.
CLKOUT	B5/8m	17	24	25 MHz Clock Output 25 MHz clock source for Ethernet PHYs CLKOUT is input direction during chip reset stage used to bootstrap the mode setting to decide the 25 MHz Clock Output enable configuration, please refer to Section 3.1.
NC	P	41	68, 63, 33	Reserved. Please connect to GND.

Table 1-2: Ethernet PHY Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
P0_TXOP	AB	36	60	PHY 0 differential Transmitted Positive signal In the copper mode, the differential data is transmitted to the media on the TXOP/TXON signal pair in the MDI mode. In the fiber mode, the signal pair should be connected to the TX+/TX- pin of the fiber transceiver.
P0_TXON	AB	35	59	PHY 0 differential Transmitted Negative signal
P0_RXIP	AB	34	56	PHY 0 differential Received Positive signal In the copper mode, the differential data from the media is received on the RXIP/RXIN signal pair in the MDI mode. In the fiber mode, the signal pair should be connected to the RX+/RX- pin of the fiber transceiver.
P0_RXIN	AB	33	55	PHY 0 differential Received Negative signal
P0_SD	AB	32	52	PHY 0 fiber mode Signal Detect SD < 0.2V, Copper mode- 1.0V < SD < 1.8V, Fiber mode without detected signal. Generate far-end fault SD > 2.4V, Fiber mode with detected signal
P0_ACT\ P0_FIBER	B5/4m	76	122	PHY 0 Link/Activity LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the PHY 0 media mode, please refer to Section 3.1.
P1_TXOP	AB	22	36	PHY 1 differential Transmitted Positive signal Same as PHY0 TXOP/ON description
P1_TXON	AB	23	37	PHY 1 differential Transmitted Negative signal
P1_RXIP	AB	24	40	PHY 1 differential Received Positive signal Same as PHY0 RXIP/IN description
P1_RXIN	AB	25	41	PHY 1 differential Received Negative signal
P1_SD	AB	26	44	PHY 1 fiber mode Signal Detect Same P0_SD description
P1_ACT\ P1_FIBER	B5/4m	74	119	PHY 1 Link/Activity LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the PHY 1 media mode, please refer to Section 3.1.
RSET_BG	AO	27	45	PHY off-chip Bias Resistor Connects an external resistor of 12 KΩ ± 1% to the PCB analog ground.

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Table 1-3: Power/Ground Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
VCC3IO	P	69, 57, 51, 16, 1	113, 91, 80, 23, 1	Digital Power for I/O pins, 3.3V Please add a 0.1uF bypass capacitor between each VCC3IO and GND.
VCCK	P	73, 50, 2	117, 79, 49, 2	Digital Power for core, 1.2V Please add a 0.1uF bypass capacitor between each VCCK and GND.
VCC33A	P	31, 28	51, 46	Analog Power for Ethernet PHY, 3.3V Please add a 0.1uF bypass capacitor between VCC33A and GND.
VCC33A_XTAL	P	40	67	Analog Power for XTAL, 3.3V Please add a 0.1uF bypass capacitor between VCC33A and GND.
VCC12A	P	30, 29	50, 47	Analog Power for Ethernet PHY, 1.2V Please add a 0.1uF bypass capacitor between VCC12A and GND.
VCC12A_PLL	P	37	64	Analog Power for PLL, 1.2V. Please add a 0.1uF bypass capacitor between VCC12A_PLL and GND.
GND	P	EPAD	EPAD, 48	Ground for all Analog and Digital Power.
GNDA	P	-	62, 61, 58, 57, 54, 53, 43, 42, 39, 38, 35, 34	Analog Ground

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1.4.2 PDI Digital IO / GPIO

Table 1-4: PDI Digital I/O, GPIO Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
IO[63:56]	B5/T/8m	N/A	32, 30, 28, 26, 128, 124, 121, 118	Digital/General Purpose I/O[63:56]
IO[55:48]	B5/T/8m	N/A	84, 82, 78, 76, 21, 19, 17, 15	Digital/General Purpose I/O[55:48]
IO[47:40]	B5/T/8m	N/A	13, 11, 9, 112, 110, 108, 106, 104	Digital/General Purpose I/O[47:40]
IO[39:32]	B5/T/8m	N/A	102, 100, 90, 88, 86, 97, 93, 95	Digital/General Purpose I/O[39:32]
IO[31:24]	B5/T/8m	21, 20, 19, 18, 15, 77, 75, 71	31, 29, 27, 25, 22, 123, 120, 115	Digital/General Purpose I/O[31:24]
IO[23:16]	B5/T/8m	53, 52, 49, 48, 14, 13, 12, 11	83, 81, 77, 75, 20, 18, 16, 14	Digital /General Purpose I/O[23:16]
IO[15:8]	B5/T/8m	10, 9, 8, 68, 67, 66, 65, 64	12, 10, 8, 111, 109, 107, 105, 103	Digital /General Purpose I/O[15:8]
IO[7:0]	B5/T/8m	63, 62, 56, 55, 54, 60, 58, 59	101, 99, 89, 87, 85, 96, 92, 94	Digital /General Purpose I/O[7:0]
SOF	O5/8m	7	7	Start-of-Frame
EOF	O5/8m	3	3	End-of-Frame
OE_EXT	I5	5	5	Output Enable
OUTVLD	O5/8m	4	4	Output data Valid/Output event
LAT_IN	I5	6	6	external data Latch
WD_TRIG	O5/8m	80	127	Watchdog Trigger

Note: The IO[63:0] in PDI Digital mode is for DIO[63:0], in PDI SPI slave mode is for GPIO[63:0], **and the IO[63:0] are the tri-stateable.**

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1.4.3 ESC PDI / Function SPI Slave Interface

Table 1-5: PDI SPI Slave Interface Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
SCS_ESC	I5	7	7	SPI Chip Select for ESC
SCS_FUNC	I5	3	3	SPI Chip Select for Function
SCLK	I5	5	5	SPI Clock share pin for ESC and Function
MOSI	I5	4	4	SPI data MOSI share pin for ESC and Function
MISO	O5	6	6	SPI data MISO share pin for ESC and Function
SINT	O5/T	80	127	SPI Interrupt share pin for ESC and Function

Note 1: The Function SPI slave could share pin with ESC or use independent pin, please refer to Section 3.2.
Note 2: "Function" means the design for PWM, Incremental/Hall Encoder, SPI Master, I/O Watchdog and excluding ESC.

1.4.4 ESC PDI / Function Local Bus Interface

Table 1-6: PDI Local Bus Interface Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
LECSn	I5	7	7	Local bus ESC Chip Select
LFCSn	I5	3	3	Local bus Function Chip Select
LRDn	I5	5	5	Local bus Read
LWRn	I5	4	4	Local bus Write
LBHE	I5	52	81	Local bus Byte High Enable (16-bit width only)
LRDY	O5/T	6	6	Local bus Ready
LINT	O5/T	80	127	Local bus Interrupt
LALE	I5	53	83	LB Address Latch Enable
LA[13:0]	I5	49, 48, 14, 13, 12, 11, 10, 9, 8, 68, 67, 66, 65, 64	77, 75, 20, 18, 16, 14, 12, 10, 8, 111, 109, 107, 105, 103	Local bus Address bus
LDA[15:8]	B5	21, 20, 19, 18, 15, 77, 75, 71	31, 29, 27, 25, 22, 123, 120, 115	Local bus Data bus [15:8]
LDA[7:0]	B5	63, 62, 56, 55, 54, 60, 58, 59	101, 99, 89, 87, 85, 96, 92, 94	Local bus Data bus [7:0]

Note: "Function" means the design for PWM, Incremental/Hall Encoder, SPI Master, I/O Watchdog and excluding ESC.

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1.4.5 PWM Motor Controller

Table 1-7: PWM Motor Controller Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
PWM1L	O5/T	15	128	PWM 1 Low pin or STEP pin
PWM1H	O5/T	77	124	PWM 1 High pin or DIR pin
PWM2L	O5/T	75	121	PWM 2 Low pin
PWM2H	O5/T	71	118	PWM 2 High pin
PWM3L	O5/T	53	84	PWM 3 Low pin
PWM3H	O5/T	52	82	PWM 3 High pin
PULA	O5	14	21	Pulse A, programmable point A
PULB	O5	13	19	Pulse B, programmable point B
PULZ	O5	49	78	Pulse Z, PWM period start point
PULC	O5	48	76	Pulse C, PWM period central point
PULAB	O5	12	17	Pulse AB, toggle when programmable point A and B
EMn	I5	18	26	Emergency input, active low

1.4.6 Incremental / Hall Encoder Interface

Table 1-8: Incremental/Hall Encoder Interface Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
ENCA	I5	19	28	ENC input A, Sin., CW, CLK, or HALL A
ENCB	I5	20	30	ENC input B, Cos., CCW, DIR, or HALL B
ENCZ	I5	21	32	ENC input Z, Zero point or HALL C

1.4.7 SPI Master

Table 1-9: SPI Master Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
MSS[3:0]	O5	63, 62, 56, 55	102, 100, 90, 88	SPI Master Slave Select
MSCLK	O5	59	95	SPI Master SCLK
MMOSI	O5	58	93	SPI Master MOSI
MMISO	I5	60	97	SPI Master MISO
MINT	I5	54	86	SPI Master Interrupt in
MTRG	I5	65	106	SPI Master Trigger in
MDRLD	B5	64	104	SPI Master ADC Data Ready / DAC Data Loaded

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1.4.8 3/4 Port MII

Table 1-10: Port 2 or Port 0 MII Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
CLKOUT	O5	17	24	Clock Output 25 MHz clock output This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the CLKOUT output driving, please refer to Section 3.1.
MCLK	B5	10	13	MII Clock 25 MHz clock source for Ethernet PHYs This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the MCLK output driving, please refer to Section 3.1.
MDC	O5	11	15	PHY Management Interface clock
MDIO	B5	12	17	PHY Management Interface data
P2_LINK	I5	53	84	LINK Provided by the PHY if a 100 Mbps (Full Duplex) link is established.
P2_TXD[3] \ SWAP_P0	O5	49	78	Transmit data [3]. Transmit data [3] is input direction during chip reset stage used to bootstrap the mode setting to decide the Port 0 MII enable configuration, please refer to Section 3.1.
P2_TXD[2:1] \ TX_SH[1:0]	O5	48, 14	76, 21	Transmit data [2:1] This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the external PHY's TXD phase shift, please refer to Section 3.1.
P2_TXD[0] \ LINK_POL	O5	13	19	Transmit data [0] These pins are input direction during chip reset use to bootstrap the mode setting to decide external PHY's LINK polarity, please refer to Section 3.1.
P2_TX_EN \ 4PORT_MODE	O5	52	82	Transmit enable. Transmit enable is input direction during chip reset stage used to bootstrap the mode setting to decide the MII 4th enable configuration, please refer to Section 3.1.
P2_RX_CLK	I5	20	30	Receive Clock
P2_RXD[3:0]	I5	15, 77, 75, 71	128, 124, 121, 118	Receive data
P2_RX_ER	I5	19	28	Receive error
P2_RX_DV	I5	18	26	Receive data valid
P2_ACT	O5	21	32	Link/Activity LED

Table 1-11: Port 3 MII Pin Description

Pin Name	Type	Pin No		Pin Description
		LQFP80	LQFP128	
P3_LINK	I5	9	11	LINK Provided by the PHY if a 100 Mbps (Full Duplex) link is established.
P3_TXD[3]	O5	68	112	Transmit data [3]
P3_TXD[2:1] \ P3_TX_SH[1:0]	O5	67, 66	110, 108	Transmit data [2:1] This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the external PHY's TXD phase shift, please refer to Section 3.1.

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P3_TXD[0] \ P3_LINK_POL	O5	65	106	Transmit data [0] These pins are input direction during chip reset use to bootstrap the mode setting to decide external PHY's LINK polarity, please refer to Section 3.1.
P3_TX_EN	O5	8	9	Transmit enable
P3_RX_CLK	I5	64	104	Receive Clock
P3_RXD[3:0]	I5	56, 55, 54, 60	90, 88, 86, 97	Receive data
P3_RX_ER	I5	62	100	Receive error
P3_RX_DV	I5	63	102	Receive data valid
P3_ACT	O5	58	93	Link/Activity LED

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2 Function Description

2.1 Clocks/Resets

The AX58101(2) requires a crystal (25MHz, ±25 PPM at room temperature) as the clock source. Internal PLL generates the 100MHz clock for EtherCAT SubDevice Controller (ESC) and also for other functions.

The AX58101(2) has three reset sources. First, during the VCCK power-on, the internal Power-On-Reset (POR) can generate a reset pulse to reset all the function blocks when the VCCK power pin rises to a certain threshold voltage level. The second reset is RSTn pin, which is to do the fundamental reset. And third, EtherCAT command reset, the EtherCAT MainDevice can send reset sequence to force AX58101(2) reset. AX58101(2) also supports a reset output RSTO polarity bootstrap configuration (RSTO_POL).

2.2 EtherCAT SubDevice Controller (ESC)

The AX58101(2) implements a 3/4 port EtherCAT SubDevice controller (ESC), licensed from Beckhoff Automation, with 9 Kbytes Process Data RAM, 8 Fieldbus Memory Management Units (FMMUs), 8 Sync-Managers and a 64-bit Distributed Clock.

Port 0 and 1 integrate embedded Ethernet PHYs, and port 2/3 is an optional MII interface which are multi-function pins shared with other interfaces (i.e. PWM, Hall, Local Bus, Digital I/O). Packets are forwarded in the following order: **Port 0->EtherCAT Processing Unit->Port 3->Port 1->Port 2**.

The Process Data Interface (PDI, also named host interface) provides SPI slave, asynchronous 8/16-bit microcontroller interface (also named Asynchronous Local Bus) and Digital I/O. The SPI slave and asynchronous 8/16-bit Local Bus interface will be used when external MCU in employed the slave system, and the Digital I/O is used for when direct I/O control.

For detailed information about the EtherCAT technology, the EtherCAT core mechanisms, and major features, we refer to the official standard documentations and guidelines available from ETG (www.ethercat.org, ETG.1000), IEC (http://www.iec.ch, IEC61158, IEC61784-2, IEC 61800-7), and Beckhoff (http://www.beckhoff.de, technical specification) web sites.

2.3 Ethernet PHY

The AX58101(2) is embedded two DSP-based Ethernet PHYs, which are fully compliant with the 100BASE-TX and 100BASE-FX Ethernet standards such as IEEE 802.3u, and ANSI X3.263-1995 (FDDI-TP-PMD). In copper mode, it supports the MDI/MDIX auto-crossover function (HP Auto-MDIX).

2.4 I/O Watchdog

The I/O Watchdog is for AX58101(2) safety engine and used to monitor I/O signals toggle status and an emergency stop input (EMn) pin. When I/O signals don't match a pattern or keep over excepted time, the watchdog will be triggered, or EMn input pin asserted which would force I/O pads to enter default level. The default level is configurable which could be driven low, high or Tristate.

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2.5 PWM Controller

The PWM control module provides Pulse Width Modulation (PWM) and STEP / DIR to control motor driving. The PWM mode has eight pins. There are three pairs of control signal. Each control signal pair has a high pulse pin (PWMxH) and low pulse pin (PWMxL) control power drive circuit. Others are two alignment pins, PULZ and PULC point cycle start and central time, and three programmable trigger pins, PULA PULB and PULAB. The step pulse mode has 2 pins, step (STEP) and direction (DIR), which connect to step motor controller and share PWM1H/L pins.

The PWM supports up to 12.5MHz output frequency, and programmable polarity, timing adjustment.

2.6 Incremental and Hall Encoder Interface

The AX58101(2) provides an interface with a linear or rotary incremental encoder to get position information, and supports four input modes, including the Sin/Cos mode (A / B / Z pins), Clock-Wise mode (CW / CCW / Z pins), Direction-Clock mode (DIR / CLK / Z pins) and the Hall mode (A / B / C pins). It can accumulate positions in three modes, Sin/Cos, Clock-Wise and Direction-Clock modes, and calculate the GAP time in Hall mode.

The Sin/Cos mode supports input frequency up to 8.33MHz, CW/CCW and DIR/CLK up to 16.66MHz, and the Hall mode up to 2.77MHz respectively.

2.7 SPI Master Controller

The Serial Peripheral Interface (SPI) master controller provides a full-duplex, synchronous serial communication interface (4 wires) to flexibly work with numerous SPI peripheral devices or microcontroller with the SPI slave. The SPI master controller supports 4 types of interface timing modes, namely, mode 0, 1, 2, and 3 to allow working with most SPI devices available. It also supports MSB/LSB first data transfer.

The SPI master controller supports 8 channels, which could sequentially access per device, and supports variable transfer length up to 8 bytes each channel. It also supports multi-channel access to the same device, and the data length could be up to 64bytes. For high performance applications, the SPI master controller supports continuous transfer data between the SPI device and data registers.

The SPI master controller provides 4 chip select, supports one-cold encode output (up to 4 devices), or uses binary encode output (use an external binary decoder) up to 8 devices.

The SPI master controller supports standard SPI device access without glue logic circuit. Besides, it supports “trigger data ready input” for ADC application, and also supports “data loaded indication out” and “data path daisy chain” for DAC application.

The MSCLK (SPI clock) is programmable by software and can run up to 50MHz.

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3 Chip Configuration and Memory Map Description

3.1 Bootstrap Pins for Chip Configuration

The AX58101(2) supports multi-function bootstrap pins for four classifications of hardware configurations, i.e. external I^2C EEPROM size, ESC supported port number, RSTO polarity and integrated port 0/1 PHY media mode; and it also supports the three and four ESC port multi-function bootstrap pins for the configuration of port 2/3 MII signals, and additional support the ESC port 0 and port 2 interface swap function. User needs to utilize an external resistor to pull up (1) / down (0) these bootstrap pins.

3.1.1 Bootstrap Pins Configuration for General

Table 3-1: Bootstrap Pins Configuration for General

Pins		Signal Name	Description
LQFP80	LQFP128		
79	126	EEP_SIZE	I^2C EEPROM Size 0: 1 Kbit to 16Kbit 1: 32Kbit to 4Mbit
44	71	RSTO_POL	RSTO Reset Output Polarity 0: Active Low 1: Active High
45	72	PDI_EMU	Device emulation (0x0141.0) 0: Device status register is controlled by PDI 1: Device status register is identical to device control register
17	24	CLKOUT	CLKOUT Enable 0: Disable CLKOUT 1: Enable CLKOUT
10	13	MCLK	MCLK and CLKOUT Driving Select: 0: 4mA 1: 8mA
52	82	4PORT_MODE	ESC port number, 4PORT_MODE is MSB and 3PORT_MODE is LSB 2'b00: 2 ports mode 2'b01: 3 ports mode 2'b10: Reserved 2'b11: 4 ports mode Notice: The 3PORT_MODE must be 1 when 4PORT_MODE set 1
78	125	3PORT_MODE	
49	78	SWAP_P0	MII interface port selection 0: Select MII2 port to IO 1: Select MII0 port to IO Notice: actives while 3PORT_MODE is set, and ESC port 0 sets the MII.
48	76	Px_TX_SH [1]	Port x MII TXD Align position 2'b00: Align with MCLK, 2'b01: Delay 1/4 phase with MCLK 2'b10: Delay 1/2 phase with MCLK 2'b11: Delay 3/4 phase with MCLK Notice: x mane 0 or 2, and actives while 3PORT_MODE is set
14	21	Px_TX_SH [0]	
13	19	Px_LINK_POL	Port 2 MII LINK Polarity 0: Active Low

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			1: Active High Notice: x mane 0 or 2, and actives while 3PORT_MODE is set
67	110	P3_TX_SH [1]	Port 3 MII TXD Align position 2‘b00: Align with MCLK, 2’b01: Delay 1/4 phase with MCLK 2’b10: Delay 1/2 phase with MCLK 2’b11: Delay 3/4 phase with MCLK Notice: these actives while 3PORT_MODE and 4PORT_MODE are set
66	108	P3_TX_SH [0]	
65	106	P3_LINK_POL	Port 3 MII LINK Polarity 0: Active Low 1: Active High Notice: these actives while 3PORT_MODE and 4PORT_MODE are set

3.1.2 Bootstrap Pins Configuration for PHY’s Fiber Mode

Table 3-2: Bootstrap Pins Configuration for PHY’s Fiber Mode

Pins		Signal Name	Description
LQFP80	LQFP128		
72	116	EPE_PDI [2]	PHY’s Fiber Mode Must be Condition 3’b000, 3’b010, 3’b011: Fiber mode must be condition Others: Reserved Note: Using the fiber mode the PDI only choose SPI, LB 8/16 bits mode.
70	114	EPE_PDI [1]	
79	126	EPE_PDI [0]	
76	122	P0_FIBER	Port 0 PHY media mode 0: Copper mode 1: Fiber mode
74	119	P1_FIBER	Port 1 PHY Media mode 0: Copper mode 1: Fiber mode

Note: While the fiber mode is enabled, the “EEPROM PDI Access State” register bit 0 is set “1” by hardware.

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3.1.3 Bootstrap Pins Configuration for None EEPROM Load

The AX58101(2) support the PDI selection without EEPROM mode, that can provide two types (SPI and asynchronous local bus) PDI, and detail configuration as Table 3-3.

Table 3-3: Bootstrap Pins Configuration for None EEPROM Load

Pins		Signal Name	Description
LQFP80	LQFP128		
72	116	EPE_PDI [2]	PDI select 3'b000: PDI selected SPI 3'b010: PDI selected Asynchronous Local Bus 8bit Mode 3'b011: PDI selected Asynchronous Local Bus 16bit Mode 3'b11x: Disable PDI select with none EEPROM load Other: Reserved
70	114	EPE_PDI [1]	
79	126	EPE_PDI [0]	
80	127	EPE_INT	Interrupt setting without EEPROM Load 1: OD, active low, edge trig 0: OS, active high, edge trig
47	74	EPE_SPI [2]	Data Out sample mode: 0: Normal sample 1: Late sample
6	6	EPE_SPI [1]	SPI mode: 2'b00: mode0 2'b01: mode1 2'b10: mode2 2'b11: mode3
4	4	EPE_SPI [0]	
63	101	EPE_LB [7]	AD_Merge for Asynchronous Local Bus: 0: AD separate 1: AD Merge
62	99	EPE_LB [6]	LALE polarity for Asynchronous Local Bus: 0: Active low 1: Active High
56	89	EPE_LB [5]	Read BUSY delay for Asynchronous Local Bus: 0: Normal read BUSY output 1: Delay read BUSY output
55	87	EPE_LB [4]	RD Polarity for Asynchronous Local Bus: 0: Active low 1: Active High
54	85	EPE_LB [3]	Perform internal write at for Asynchronous Local Bus: 0: End of write access 1: Beginning of write access
60	96	EPE_LB [2]	BUSY output driver/polarity for Asynchronous Local Bus: 2'b00: Push-Pull active low 2'b01: Open Drain (active low) 2'b10: Push-Pull active high 2'b11: Open Source (active high)
58	92	EPE_LB [1]	
59	94	EPE_LB [0]	BHE Polarity for Asynchronous Local Bus 0: Active Low 1: Active High

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3.2 Hardware Configuration EEPROM (HWCFGEE)

The AX58101(2) I²C master controller supports the communication to external I²C devices and an I²C Hardware Configuration EEPROM Loader to support loading the EtherCAT SubDevice Information (ESI) from external I²C EEPROM during chip reset. The AX58101(2) supports I²C EEPROM with EEPROM size from 1 Kbit (128 bytes) to 4 Mbit (500Kbytes).

The AX58101(2) I2C Hardware Configuration EEPROM layout is shown in following figure.

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
ESC Configuration Area			
0x00	0x00	PDI Control	0x0140
0x01		ESC Configuration (bit 2 is also mapped to ESC register 0x0110.2)	0x0141
0x02	0x01	PDI Configuration	0x0150
0x03		Sync/Latch [1:0] Configuration	0x0151
0x05 - 0x04	0x02	Pulse Length of SyncSignals	0x0983 - 0x0982
0x07 - 0x06	0x03	Extended PDI Configuration	0x0153 - 0x0152
0x09 - 0x08	0x04	Configured Station Alias	0x0013 - 0x0012
0x0A	0x05	Host Interface Extend Setting and Drive Strength	
0x0B		Reserved, shall be zero	
0x0C	0x06	Reserved, shall be zero	
0x0D		Multi-Function Select and Drive Strength	
0x0F - 0x0E	0x07	Checksum	
0x13 - 0x10	0x09 – 0x08	Vendor ID	
0x17 - 0x14	0x0B – 0x0A	Product Code	
0x1B - 0x18	0x0D – 0x0C	Revision Number	
0x1F - 0x1C	0x0F – 0x0E	Serial Number	
0x27 - 0x20	0x13 – 0x10	Reserved	
Bootstrap Mailbox Config			
0x29 - 0x28	0x14	Bootstrap Receive Mailbox Offset	
0x2B - 0x2A	0x15	Bootstrap Receive Mailbox Size	
0x2D - 0x2C	0x16	Bootstrap Send Mailbox Offset	
0x2F - 0x2E	0x17	Bootstrap Send Mailbox Size	
Mailbox Sync Man Config			
0x31 - 0x30	0x18	Standard Receive Mailbox Offset	
0x33 - 0x32	0x19	Standard Receive Mailbox Size	
0x35 - 0x34	0x1A	Standard Send Mailbox Offset	
0x37 - 0x36	0x1B	Standard Send Mailbox Size	
0x39 - 0x38	0x1C	Mailbox Protocol	
0x3F - 0x3A	0x1F – 0x1D	Reserved	
0x7B - 0x40	0x3D – 0x20	Reserved	
0x7D - 0x7C	0x3E	Size	
0x7F - 0x7E	0x3F	Version	
ESC Category 1 (for AX58101(2) Enhance Access Configuration if used) *Note1			
0x81 ~ 0x80	0x40	Category 1 Type (Default: **0x0001**)	
0x83 ~ 0x82	0x41	Category 1 Data Size (words) (Default: **0x0021**)	
0x84 ~0x85	0x42	Drive Strength	

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EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
0x86 ~ 0x87	0x43	Extended PDI Configuration High	
Other ESC Categories Information (Subdivided in Categories)			
		…	
		Category Strings	
		Category Generals	
		Category FMMU	
		Category SyncManager	
		Category Tx - / RxPDO for each PDO	

Figure 3-1: AX58101(2) I²C EEPROM Layout

Note 1: Reserved words or reserved bits of the ESC Configuration Area should be filled with 0.

Note 2: When (re-) configuring the EEPROM from an EtherCAT MainDevice system special care must be taken. Not every master allows writing a category 1 entry to the EEPROM. There are different ways to write this into the EEPROM for automatically loading access control configuration when AX58101(2) booting.

1. Use preprogrammed I²C EEPROM.
2. Use a different category, e.g., 2049, first. Then overwrite the upper byte with 0 with a single EEPROM byte writes.

The AX58101(2) HWCFGEE contents from offset 0x00 to 0x7F are mandatory, as well as the general category (at least the minimum I2C EEPROM size is 2Kbit, and for the complex devices with many categories should be equipped with 32 Kbit EEPROMs or larger one). The ESC Configuration Area is used for AX58101(2) hardware configuration. All other areas are used by the EtherCAT MainDevice or the local application.

The ESC Configuration Area (EEPROM offset 0x00 to 0x0F) is automatically read by AX58101(2) after power-on or reset. It contains the PDI configuration, Distributed Clocks settings, and Configured Station Alias. The consistency of the ESC Configuration Area data is secured with a checksum.

The EtherCAT MainDevice can invoke reloading the EEPROM contents. In this case, the Configured Station Alias register 0x0012:0x0013 and ESC Configuration register bits 0x0141 [1,4,5,6,7] (enhanced link detection) are not transferred into the registers. They are only transferred at the initial EEPROM loading after power-on or reset.

To use AX58101(2) configured the PHY's registers functionalities, users should define the EEPROM PHY command Configuration parameters in the first category located at EEPROM offset 0x80. The Category Type must be 0x0001and the Category Data Size value based on how many PHY's registers (configured one register needs two words) need to configure for the detail please reference Category 1 Data Size (0x83 - 0x82).

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3.2.1 EEPROM Contents Detailed Descriptions

PDI Control (0x00)

Bit	Description
7:0	PDI Control [7:0] 0x00: Interface deactivated (no PDI) 0x04: Digital I/O 0x05: SPI Slave 0x08: 16-bit Asynchronous Local Bus 0x09: 8-bit Asynchronous Local Bus 0x88: 16-bit Asynchronous Local Bus supporting address/data (A/D) merging 0x89: 8-bit Asynchronous Local Bus supporting address/data (A/D) merging Others: reserved

ESC Configuration (0x01)

Bit	Description
0	Device emulation enables (control of AL status)
1	Enhanced Link detection all ports
3:2	Reserved
4	Enhanced Link port 0
5	Enhanced Link port 1
6	Enhanced Link port 2
7	Enhanced Link port 3

PDI Configuration (0x02)

Digital I/O

Bit	Description
0	OUTVALID polarity
1	OUTVALID mode
2	Unidirectional/Bidirectional mode
3	Watchdog behavior
5:4	Input DATA is sampled
7:6	Output DATA is updated

SPI Slave

Bit	Description
1:0	SPI mode
3:2	SPI_IRQ output driver/polarity
4	SPI_SEL polarity
5	Data Out sample mode
7:6	Reserved

Asynchronous Local Bus

Bit	Description
1:0	BUSY/RDY driver/polarity
3:2	IRQ driver/polarity
4	BHE/Byte Enable polarity
7:5	Reserved

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Sync/Latch[1:0] Configuration (0x03)

Bit	Description
1:0	SYNC0 output driver/polarity
2	SYNC0/LATCH0 configuration
3	SYNC0 mapped to AL Event Request
5:4	SYNC1 output driver/polarity
6	SYNC1/LATCH1 configuration
7	SYNC1 mapped to AL Event Request

Pulse Length SyncSignals (0x05 - 0x04)

Bit	Description
15:0	Pulse length of SyncSignal

Extended PDI Configuration (0x07 - 0x06)

Digital I/O / SPI Slave (for GPIO)

Bit	Description
0	Digital I/O or GPIO Digital I/O or GPIO are configured in pairs (1:0) as inputs or outputs: 0: Input 1: Output
1	3:2 pair (0: Input, 1: Output)
2	5:4 pair (0: Input, 1: Output)
3	7:6 pair (0: Input, 1: Output)
4	9:8 pair (0: Input, 1: Output)
5	11:10 pair (0: Input, 1: Output)
6	13:12 pair (0: Input, 1: Output)
7	15:14 pair (0: Input, 1: Output)
8	17:16 pair (0: Input, 1: Output)
9	19:18 pair (0: Input, 1: Output)
10	21:20 pair (0: Input, 1: Output)
11	23:22 pair (0: Input, 1: Output)
12	25:24 pair (0: Input, 1: Output)
13	27:26 pair (0: Input, 1: Output)
14	29:28 pair (0: Input, 1: Output)
15	31:30 pair (0: Input, 1: Output)

Asynchronous Local Bus

Bit	Description
0	Read BUSY delay
1	Perform internal write
2	LALE polarity 0: Active Low 1: Active High
3	Reserved
4	9:8 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
5	11:10 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
6	13:12 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
7	15:14 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
8	17:16 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
9	19:18 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
10	21:20 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
11	23:22 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
12	25:24 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
13	27:26 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)

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14	29:28 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)
15	31:30 pair (A/D merge mode and data bus 8-bit width only) (0: Input, 1: Output)

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Configured Station Alias (0x09 - 0x08)

Bit	Description
15:0	Alias Address used for node addressing

Host Interface Extend Setting and Drive Strength (0x0A)

Digital I/O

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>4:0</td><td>Reserved</td></tr>
<tr><td>5</td><td>Control Driving Select:
0: 4mA
1: 8mA</td></tr>
<tr><td>6</td><td>IO [9:0] or IO [41:32] Driving Select:
0: 4mA
1: 8mA
<table>
<tr><td rowspan="2">IO</td><td colspan="2">LQFP80</td><td colspan="2">QFP128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>IO [9:0]</td><td>4mA</td><td>8mA</td><td colspan="2">Config by Category 1</td></tr>
<tr><td>IO [41:32]</td><td colspan="2">off</td><td>4mA</td><td>8mA</td></tr>
</table></td></tr>
<tr><td>7</td><td>IO [15:10] or IO [48:42] Driving Select:
0: 4mA
1: 8mA
<table>
<tr><td rowspan="2">IO</td><td colspan="2">LQFP80</td><td colspan="2">QFP128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>IO [16:10]</td><td>4mA</td><td>8mA</td><td colspan="2">Config by Category 1</td></tr>
<tr><td>IO [48:42]</td><td colspan="2">off</td><td>4mA</td><td>8mA</td></tr>
</table></td></tr>
</table>

SPI Slave / Asynchronous Local Bus

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>3:0</td><td>Interrupt Edge Pulse Length (INTP_LEN)
Interrupt Edge Pulse = (INTP_LEN+1) * 100ns</td></tr>
<tr><td>4</td><td>The trigger type of interrupt signal, SINT / LINT
0: Level trigger.
1: Edge trigger.</td></tr>
<tr><td>5</td><td>Control Driving Select:
0: 4mA
1: 8mA</td></tr>
<tr><td>6</td><td>IO [9:0] or IO [9:0] Driving Select:
0: 4mA
1: 8mA
<table>
<tr><td rowspan="2">IO</td><td colspan="2">LQFP80</td><td colspan="2">QFP128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>IO [9:0]</td><td>4mA</td><td>8mA</td><td colspan="2">Config by Category 1</td></tr>
<tr><td>IO [41:32]</td><td colspan="2">off</td><td>4mA</td><td>8mA</td></tr>
</table></td></tr>
<tr><td>7</td><td>IO [15:10] or IO [48:42] Driving Select:
0: 4mA
1: 8mA
<table>
<tr><td rowspan="2">IO</td><td colspan="2">LQFP80</td><td colspan="2">QFP128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>IO [16:10]</td><td>4mA</td><td>8mA</td><td colspan="2">Config by Category 1</td></tr>
<tr><td>IO [48:42]</td><td colspan="2">off</td><td>4mA</td><td>8mA</td></tr>
</table></td></tr>
</table>

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Multi-Function Select and Drive Strength (0x0D)

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>IO [9:0], [41:32] select:
0: IO [9:0]
1: MTRG, MDRLD, MSS [3:0], MINT, MMISO, MMOSI, MSCLK,

<table>
<tr><td rowspan="2">IO</td><td colspan="2">LQFP80</td><td colspan="2">QFP128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>IO [9:0]</td><td>DIO/GPIO [9:0]</td><td>MTRG, MDRLD, MSS[3:0], MINT, MMISO, MMOSI, MSCLK</td><td colspan="2">DIO/GPIO [9:0]</td></tr>
<tr><td>IO [41:32]</td><td colspan="2">NA</td><td>DIO/GPIO [41:32]</td><td>MTRG, MDRLD, MSS[3:0], MINT, MMISO, MMOSI, MSCLK</td></tr>
</table>
Note: when LQFP80 in Local Bus mode this bit no function</td></tr>
<tr><td>1</td><td>IO [19:17] (PUL AB) select:
0: IO [19:17]
1: PULA, PULB, PULAB

<table>
<tr><td rowspan="2">IO</td><td colspan="2">LQFP80</td><td colspan="2">QFP128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>IO [19:17]</td><td>DIO/GPIO [19:17]</td><td>PULA, PULB, PULAB</td><td colspan="2">DIO/GPIO [19:17]</td></tr>
<tr><td>IO [51:49]</td><td colspan="2">NA</td><td>DIO/GPIO [51:49]</td><td>PULA, PULB, PULAB</td></tr>
</table>
Note: when LQFP80 in Local Bus mode this bit no function</td></tr>
<tr><td>2</td><td>IO [21:20] select (PUL ZC):
0: IO [21:20]
1: PULZ, PULC

<table>
<tr><td rowspan="2">IO</td><td colspan="2">LQFP80</td><td colspan="2">QFP128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>IO [21:20]</td><td>DIO/GPIO [21:20]</td><td>PULZ, PULC</td><td colspan="2">DIO/GPIO [21:20]</td></tr>
<tr><td>IO [53:52]</td><td colspan="2">NA</td><td>DIO/GPIO [53:52]</td><td>PULZ, PULC</td></tr>
</table>
Note: in Local Bus mode this bit no function</td></tr>
<tr><td>3</td><td>IO [25:22] select (PWM23):
0: IO [25:22]
1: PWM2L, PWM2H, PWM3L, PWM3H

<table>
<tr><td rowspan="2">IO</td><td colspan="2">LQFP80</td><td colspan="2">QFP128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>IO [25:22]</td><td>DIO/GPIO [25:22]</td><td>PWM2L, PWM2H, PWM3L, PWM3H</td><td colspan="2">DIO/GPIO [25:22]</td></tr>
<tr><td>IO [57:54]</td><td colspan="2">NA</td><td>DIO/GPIO [57:54]</td><td>PWM2L, PWM2H, PWM3L, PWM3H</td></tr>
</table>
Note: when LQFP80 in Local Bus 16 bits mode this bit no function</td></tr>
<tr><td>4</td><td>IO [28:26] select (PWM1, EM):
0: IO [28:26]</td></tr>
</table>

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1: EM, PWM1L, PWM1H

IO	LQFP80		QFP128	
	0	1	0	1
IO [28:26]	DIO/GPIO [28:26]	EM, PWM1L, PWM1H	DIO/GPIO [28:26]	
IO [60:58]	NA		DIO/GPIO [60:58]	EM, PWM1L, PWM1H

Note: when LQFP80 in Local Bus 16 bits mode this bit no function

5

IO [31:29] select (ENC):
0: IO [31:29]
1: ENCZ, ENCB, ENCA

IO	LQFP80		QFP128	
	0	1	0	1
IO [31:29]	DIO/GPIO [31:29]	ENCZ, ENCB, ENCA	DIO/GPIO [31:29]	
IO [63:61]	NA		DIO/GPIO [63:61]	ENCZ, ENCB, ENCA

Note: when LQFP80 in Local Bus 16 bits mode this bit no function

6

IO [21:16] Driving Select:
0: 4mA
1: 8mA

IO	LQFP80		QFP128	
	0	1	0	1
IO [21:17]	4mA	8mA	Config by Category 1	
IO [53:49]	off		4mA	8mA

7

IO [31:22] Driving Select:
0: 4mA
1: 8mA

IO	LQFP80		QFP128	
	0	1	0	1
IO [31:22]	4mA	8mA	Config by Category 1	
IO [63:54]	off		4mA	8mA

Note for LQFP80: When 3 port mode enable, the IO [31:15] pins are forced to MII port 2, when 4-port mode enable, the IO [14:1] pins are forced to MII port3

Note for LQFP128: When 3 port mode enable, the IO [63:47] pins are forced to MII port 2, when 4-port mode enable, the IO [46:33] pins are forced to MII port3

Note for Ext-PHY mode: this mode only available on LQFP128, the IO [63:47] pins are forced to MII port0, the IO [46:33] pins are forced to MII port1, the IO [31:18] pins are forced to MII port2, the IO [14:1] pins are forced to MII port3

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Checksum (0x0F - 0x0E)

Bit	Description
15:0	Checksum Low byte contains remainder of division of EEPROM offset 0x00 to 0x0D as unsigned number divided by the polynomial X^8+X^2+X+1 (initial value 0xFF) For debugging purposes, it is possible to disable the checksum validation with a checksum value of 0x88A4. **Note that NEVER use this for production!**

Category 1 Type (0x81 - 0x80)

Bit	Description
15:0	Category 1 Type MUST be 0x0001

Category 1 Data Size (0x83 - 0x82)

Bit	Description
15:0	Category 1 Data Size (words) The "Category 1 Data Size" is decided on: For 80 pins Without PHY's registers configures, this value must be 0x0000. With PHY's registers configures (configures one register needs 2 words), if 3 registers need to configure, this value must be 0x0006 (0x0006 =3*0x2). For 128 pins Without PHY's registers configures, this value must be 0x0002. With the PHY's registers (configures one register needs 2 words), if 2 registers need and then this value is 0x0006 (0x0006 =2*0x2+0x2)

Drive Strength (0x84 – 0x85)

Bit	Description
0	IO [9:0] Driving Select at QFP128 package 0: 4ma 1: 8ma
1	IO [16:10] Driving Select at QFP128 package 0: 4ma 1: 8ma
2	IO [21:17] Driving Select at QFP128 package 0: 4ma 1: 8ma
3	IO [31:22] Driving Select at QFP128 package 0: 4ma 1: 8ma
15:4	Reserved

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Extended PDI configuration High (0x87 – 0x86)

Bit	Description
0	Digital I/O or GPIO are configured in pairs (1:0) as inputs or outputs (only for the AX58102): 33:32 pair (0: Input, 1: Output)
1	35:34 pair (0: Input, 1: Output)
2	37:36 pair (0: Input, 1: Output)
3	39:38 pair (0: Input, 1: Output)
4	41:40 pair (0: Input, 1: Output)
5	43:42 pair (0: Input, 1: Output)
6	45:44 pair (0: Input, 1: Output)
7	47:46 pair (0: Input, 1: Output)
8	49:48 pair (0: Input, 1: Output)
9	51:50 pair (0: Input, 1: Output)
10	53:52 pair (0: Input, 1: Output)
11	55:54 pair (0: Input, 1: Output)
12	57:56 pair (0: Input, 1: Output)
13	59:58 pair (0: Input, 1: Output)
14	61:60 pair (0: Input, 1: Output)
15	63:62 pair (0: Input, 1: Output)

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3.3 Memory Map

This section introduces the memory mapping in AX58101(2). AX58101(2) provides SPI and Local Bus slave interfaces for both ESC PDI and Function to access the internal registers. Section 3.3.1 introduces the ESC memory map which can be accessed by PDI SPI or Local bus interface ,and section 3.3.2 introduces the Function register map which can be accessed by Function SPI or Local Bus interface. Due to the Function registers can be accessed by PDI interface and EtherCAT MainDevice directly.

3.3.1 ESC Memory Map

Table 3-4: ESC Memory Map

ESC Address	Length (Bytes)	Description
ESC Information		
0x0000	1	Type
0x0001	1	Revision
0x0002	2	Build
0x0004	1	FMMUs supported
0x0005	1	SyncManagers supported
0x0006	1	RAM Size
0x0007	1	Port Descriptor
0x0008	2	ESC Features supported
Station Address		
0x0010	2	Configured Station Address
0x0012	2	Configured Station Alias
Write Protection		
0x0020	1	Write Register Enable
0x0021	1	Write Register Protection
0x0030	1	ESC Write Enable
0x0031	1	ESC Write Protection
Data Link Layer		
0x0040	1	ESC Reset ECAT
0x0041	1	ESC Reset PDI
0x0100	4	ESC DL Control
0x0108	2	Physical Read/Write Offset
0x0110	2	ESC DL Status
Application Layer		
0x0120	2	AL Control
0x0130	2	AL Status
0x0134	2	AL Status Code
0x0138	1	RUN LED Override
0x0139	1	ERR LED Override
PDI		
0x0140	1	PDI Control
0x0141	1	ESC Configuration
0x0150	1	PDI Configuration
0x0151	1	Sync/Latch PDI Configuration
0x0152	2	Extended PDI Configuration
Interrupts		
0x0200	2	ECAT Event Mask
0x0204	4	AL Event Mask
0x0210	2	ECAT Event Request

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0x0220	4	AL Event Request
Error Counters		
0x0300	4x2	RX Error Counter [3:0]
0x0308	4x1	Forwarded RX Error counter [3:0]
0x030C	1	ECAT Processing Unit Error Counter
0x030D	1	PDI Error Counter
0x030E	1	PDI Error Code
0x0310	4x1	Lost Link Counter [3:0]
Watchdogs		
0x0400	2	Watchdog Divider
0x0410	2	Watchdog Time PDI
0x0420	2	Watchdog Time Process Data
0x0440	2	Watchdog Status Process Data
0x0442	1	Watchdog Counter Process Data
0x0443	1	Watchdog Counter PDI
I²C EEPROM Interface		
0x0500	1	EEPROM Configuration
0x0501	1	EEPROM PDI Access State
0x0502	2	EEPROM Control/Status
0x0504	4	EEPROM Address
0x0508	4	EEPROM Data
MII Management Interface		
0x0510	2	MII Management Control/Status
0x0512	1	PHY Address
0x0513	1	PHY Register Address
0x0514	2	PHY Data
0x0516	1	MII Management ECAT Access State
0x0517	1	MII Management PDI Access State
0x0600:0x067F	**FMMU[7:0]**	
+0x0	4	Logical Start Address
+0x4	2	Length
+0x6	1	Logical Start bit
+0x7	1	Logical Stop bit
+0x8	2	Physical Start Address
+0xA	1	Physical Start bit
+0xB	1	Type
+0xC	1	Activate
+0xD	3	Reserved
0x0800:0x083F	**SyncManager[7:0]**	
+0x0	2	Physical Start Address
+0x2	2	Length
+0x4	1	Control Register
+0x5	1	Status Register
+0x6	1	Activate
+0x7	1	PDI Control
0x0900:0x09FF	**Distributed Clocks (DC)**	
DC – Receive Times		
0x0900	4	Receive Time Port 0
0x0904	4	Receive Time Port 1
0x0908	4	Receive Time Port 2
0x090C	4	Receive Time Port 3
DC – Time Loop Control Unit		

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0x0910	4(W)/8(R)	System Time
0x0918	8	Receive Time ECAT Processing Unit
0x0920	8	System Time Offset
0x0928	4	System Time Delay
0x092C	4	System Time Difference
0x0930	2	Speed Counter Start
0x0932	2	Speed Counter Diff
0x0934	1	System Time Difference Filter Depth
0x0935	1	Speed Counter Filter Depth
DC – Cyclic Unit Control		
0x0980	1	Cyclic Unit Control
DC – SYNC Out Unit		
0x0981	1	Activation
0x0982	2	Pulse Length of SyncSignals
0x0984	1	Activation Status
0x098E	1	SYNC0 Status
0x098F	1	SYNC1 Status
0x0990	8	Start Time Cyclic Operation/Next SYNC0 Pulse
0x0998	8	Next SYNC1 Pulse
0x09A0	4	SYNC0 Cycle Time
0x09A4	4	SYNC1 Cycle Time
DC – Latch In Unit		
0x09A8	1	Latch0 Control
0x09A9	1	Latch1 Control
0x09AE	1	Latch0 Status
0x09AF	1	Latch1 Status
0x09B0	8	Latch0 Time Positive Edge
0x09B8	8	Latch0 Time Negative Edge
0x09C0	8	Latch1 Time Positive Edge
0x09C8	8	Latch1 Time Negative Edge
DC – SyncManager Event Times		
0x09F0	4	EtherCAT Buffer Change Event Time
0x09F8	4	PDI Buffer Start Event Time
0x09FC	4	PDI Buffer Change Event Time
ESC specific		
0x0E00	8	Product ID
0x0E08	8	Vendor ID
Digital Input/Output		
0x0F00	4	Digital I/O Output Data
0x0F10	4	General Purpose Outputs
0x0F18	4	General Purpose Inputs
User RAM/Extended ESC features		
0x0F80	128	User RAM/Extended ESC Features
Process Data RAM		
0x1000	4	Digital I/O Input Data
0x1000	8KB	Process Data RAM

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3.3.2 Function Register Map

Table 3-5: Function Register Map

Address Offset	Name	Description
0x000	MCTLR	Motor Control Register
0x002	PXCFGR	PWM Pulse X Configure Register
0x004	PTAPPR	PWM Trigger A Pulse Position Register
0x006	PTBPPR	PWM Trigger B Pulse Position Register
0x008	PPCR	PWM Period Cycle Register
0x00A	PBBMR	PWM Pulse Break Before Make Register
0x00C	P1CTRLR	PWM1Control Register
0x00E	P1SHR	PWM1 Counter Shift Register
0x010	P1HPWR	PWM1 High Pulse Width Register
0x012	P2CTRLR	PWM2 Control Register
0x014	P2SHR	PWM2 Shift Register
0x016	P2HPWR	PWM2 High Pulse Width Register
0x018	P3CTRLR	PWM3 Control Register
0x01A	P3SHR	PWM3 Counter Shift Register
0x01C	P3HPWR	PWM3 High Pulse Width Register
0x020	SGTLR	Step Gap Time Low Register
0x022	SGTHR	Step Gap Time High Register
0x024	SHPWR	Step High Pulse Width Register
0x026	TDLYR	direction Transform Delay step Register
0x028	STNLR	Step Target Number Low Word Register
0x02A	STNHR	Step Target Number High Word Register
0x02C	SCFGR	Step Configure Register
0x02E	SCTRLR	Step Control Register
0x030	SCNTLR	Step Counter Content Low Register
0x032	SCNTHR	Step Counter Content High Register
0x034	STPSR	Step Status Register
0x038	SDGTR	Step Delta GAP Time Register
0x03A	SRMR	Step Roll Motion Register
0x040	ECNTVLR	Encoder Counter value Low Register
0x042	ECNTVHR	Encoder Counter value High Register
0x044	ECNSTLR	Encoder Constant Low Register
0x046	ECNSTHR	Encoder Constant High Register
0x048	ELATLR	Encoder Latched Low Register
0x04A	ELATHR	Encoder Latched High Register
0x04C	EMODR	Encoder Mode Configuration Register
0x04E	ECLRR	Encoder Clear Register
0x050	HALSTR	Hall State Register
0x052	EFLR	Encoder Filter Length Register
0x054	RTVLR	Reset Threshold Value Low Register
0x056	RTVHR	Reset Threshold Value High Register
0x058	LPCLLR	Last Phase Counter Latch Low Register
0x05A	LPCLHR	Last Phase Counter Latch High Register
0x05C	LZCLLR	Last Z to Z Counter Latch Low Register
0x05E	LZCLHR	Last Z to Z Counter Latch High Register
0x060	WTLR	Watchdog Timer Low Register
0x062	WTHR	Watchdog Timer High Register
0x064	WCFGR	Watchdog Configure Register
0x066	WTPVCR	Watchdog Timer Peak Value Clear Register
0x068	WMP0R	Watchdog Monitored Polarity 0 Register
0x06A	WMP1R	Watchdog Monitored Polarity 1 Register
0x06C	WMK0R	Watchdog Monitored Mask 0 Register

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0x06E	WMK1R	Watchdog Monitored Mask 1 Register
0x070	WOM0R	Watchdog Output Mask 0 Register
0x072	WOM1R	Watchdog Output Mask 1 Register
0x074	WOE0R	Watchdog Output Enable 0 Register
0x076	WOE1R	Watchdog Output Enable 1 Register
0x078	WOP0R	Watchdog Output Polarity 0 Register
0x07A	WOP1R	Watchdog Output Polarity 1 Register
0x07C	WTPVLR	Watchdog Timer Peak Value Low Register
0x07E	WTPVHR	Watchdog Timer Peak Value High Register
0x080	SPICFGR	SPI Configure Register
0x082	SPIBRR	SPI Baud Rate Register
0x084	SPIDBSR	SPI Delay Byte and SS Register
0x086	SPIDTR	SPI Delay Transfer Register
0x088	SPIRPTR	SPI RDY / Pulse Time Register
0x08A	SPILTR	SPI LDAC Time Register
0x08C	SPIPRLR	SPI Pulse/ RDY/ LDAC Register
0x090	SPI01BCR	SPI 0/1 Byte Count Register
0x092	SPI23BCR	SPI 2/3 Byte Count Register
0x094	SPI45BCR	SPI 4/5 Byte Count Register
0x096	SPI67BCR	SPI 6/7 Byte Count Register
0x098	SPI03SSR	SPI 0/1/2/3 slave Select Register
0x09A	SPI47SSR	SPI 4/5/6/7 slave Select Register
0x0A8	SPINTSR	SPI Interrupt Status Register
0x0AA	SPITSR	SPI Timeout Status Register
0x0AC	SPIPOSR	SPI Pulse Overrun Status Register
0x0AE	SPIDSR	SPI Data Status Register
0x0B0	SPIC0DR	SPI Channel 0 Data Register
0x0B8	SPIC1DR	SPI Channel 1 Data Register
0x0C0	SPIC2DR	SPI Channel 2 Data Register
0x0C8	SPIC3DR	SPI Channel 3 Data Register
0x0D0	SPIC4DR	SPI Channel 4 Data Register
0x0D8	SPIC5DR	SPI Channel 5 Data Register
0x0E0	SPIC6DR	SPI Channel 6 Data Register
0x0E8	SPIC7DR	SPI Channel 7 Data Register
0x0F0	SPIDSMR	SPI Data Status Mirror Register
0x0F2	SPIMCR	SPI Master Control Register
0x100	INTCR	Interrupt Configure Register
0x102	INTSR	Interrupt Status Register
0x104	ESTOR	ESC State Override register
0x106	HSTSR	Host interface Status Register
0x140	WMP2R	Watchdog Monitored Polarity 2 Register
0x142	WMP3R	Watchdog Monitored Polarity 3 Register
0x144	WMK2R	Watchdog Monitored Mask 2 Register
0x146	WMK3R	Watchdog Monitored Mask 3 Register
0x148	WOM2R	Watchdog Output Mask 2 Register
0x14A	WOM3R	Watchdog Output Mask 3 Register
0x14C	WOE2R	Watchdog Output Enable 2 Register
0x14E	WOE3R	Watchdog Output Enable 3 Register
0x150	WOP2R	Watchdog Output Polarity 2 Register
0x152	WOP3R	Watchdog Output Polarity 3 Register
Others	Reserved	Reserved

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4 Electrical Specifications

4.1 DC Characteristics

4.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VCCK	Digital core power supply	- 0.5 to 1.6	V
VCC3IO, VCC33A	Power supply of 3.3V I/O and Ethernet PHY	- 0.5 to 4.6	V
VCC12A_PLL	Analog power supply for PLL	- 0.5 to 1.6	V
V_{IN}	Input voltage of 3.3V I/O with 5V tolerant.	- 0.5 to 5.8	V
T_{STG}	Storage temperature.	- 65 to 150	℃
I_{IN}	DC input current.	50	mA
I_{OUT}	Output short circuit current.	50	mA

Note:
Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted in the recommended operating condition section of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

4.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Units
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
VCC33A	Analog power supply for Ethernet PHY	2.97	3.3	3.63	V
VCCK	Digital core power supply	1.08	1.2	1.32	V
VCC12A_PLL	Analog power supply for PLL	1.08	1.2	1.32	V
Tj	operating junction temperature	-40	25	125	℃
Ta	operating ambient temperature	-40	-	105	℃

4.1.3 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IN}	Input leakage current. No pull-up or pull-down.	3.3V with 5V tolerant I/O pins. Vin = VCC3IO or 0V.	-	< ±1	-	µA
C_{IN}	Input capacitance.	3.3V with 5V tolerant I/O pins.	-	2.9	-	pF
I_{OZ}	Tri-state output leakage current.	-	-	±1	-	µA

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4.1.4 DC Characteristics of 3.3V with 5V Tolerant I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC3IO	Power supply of 3.3V I/O.	3.3V I/O	2.97	3.3	3.63	V
Vil	Input low voltage.	LVTTL	-	-	0.8	V
Vih	Input high voltage.		2.0	-	-	V
Vt-	Schmitt trigger negative going threshold voltage.	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage.	Iol = 4 ~ 8mA	-	-	0.4	V
Voh	Output high voltage.	Ioh = 4 ~ 8mA	2.4	-	-	V
Vopu (1)	Output pull-up voltage for 5V tolerant IO	With internal pull-up resistor	-	2.4	-	V
Rpu	Input pull-up resistance.	Vin = 0 V	40	75	190	KΩ
Rpd	Input pull-down resistance.	Vin = VCC3IO	30	75	190	KΩ
Iin	Input leakage current.	Vin = VCC3IO or 0 V	-	±1	-	μA

Note: This parameter indicates that the pull-up resistor for the 5V tolerant I/O pins cannot reach VCC3IO DC level even without DC loading current.

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4.2 Power Consumption

This section details the device's typical supply current consumption and power dissipation.

Table 4-1: AX58101 Device only Power Consumption

Item	Conditions	VCC33A+VCC3IO	VCC12A+VCCK	Units
Digital IO (32 I/O Output)	Power on, Unlinked (Typ.)	17	24	mA
	INIT state, Linked (Typ.)	19	101	mA
	OP state, Linked (Typ.), 32 I/O driving low without any loading	21	101	mA
	OP state, Linked (Typ.) 32 I/O driving high with 510ohm + LED	87	101	mA

Note 1: The VCC33A includes VCC33A_XTAL, VCC33A_PHY0 and VCC33A_PHY1, the VCC12A includes VCC12A_PLL, VCC12A_PHY0 and VCC12A_PHY1.
Note 2: Above current value are typical values measured on AX58101 Test board.

Table 4-2: AX58101 Device and System Power Consumption

Item	Conditions	VCC33A+VCC3IO	VCC12A+VCCK	Units
Digital IO (32 I/O Output)	Power on, Unlinked (Typ.)	123	24	mA
	INIT state, Linked (Typ.)	103	101	mA
	OP state, Linked (Typ.), 32 I/O driving low without any loading	105	101	mA
	OP state, Linked (Typ.) 32 I/O driving high with 510ohm + LED	171	101	mA

Note 1: The VCC33A includes VCC33A_XTAL, VCC33A_PHY0 and VCC33A_PHY1, the VCC12A includes VCC12A_PLL, VCC12A_PHY0 and VCC12A_PHY1.
Note 2: Above current value are typical values measured on AX58101 Test board.
Note 3: "Unlinked" indicates that the PHY is not connected to an Ethernet cable and is operating in 10BASE mode.

Table 4-3: AX58102 Device only Power Consumption

Item	Conditions	VCC33A+VCC3IO	VCC12A+VCCK	Units
Digital IO (64 I/O Output)	Power on, Unlinked (Typ.)	18	24	mA
	INIT state, Linked (Typ.)	20	98	mA
	OP state, Linked (Typ.), 64 I/O driving low without any loading	23	98	mA
	OP state, Linked (Typ.) 64 I/O driving high with 510ohm + LED	144	98	mA

Note 1: The VCC33A includes VCC33A_XTAL, VCC33A_PHY0 and VCC33A_PHY1, the VCC12A includes VCC12A_PLL, VCC12A_PHY0 and VCC12A_PHY1.
Note 2: Above current value are typical values measured on AX58102 Test board.

Table 4-4: AX58102 Device and System Power Consumption

Item	Conditions	VCC33A+VCC3IO	VCC12A+VCCK	Units
Digital IO (64 I/O Output)	Power on, Unlinked (Typ.)	126	24	mA
	INIT state, Linked (Typ.)	104	98	mA
	OP state, Linked (Typ.), 64 I/O driving low without any loading	107	98	mA
	OP state, Linked (Typ.) 64 I/O driving high with 510ohm + LED	228	98	mA

Note 1: The VCC33A includes VCC33A_XTAL, VCC33A_PHY0 and VCC33A_PHY1, the VCC12A includes VCC12A_PLL, VCC12A_PHY0 and VCC12A_PHY1.
Note 2: Above current value are typical values measured on AX58102 Test board.

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Note 3: “Unlinked” indicates that the PHY is not connected to an Ethernet cable and is operating in 10BASE mode.

Table 4-5: Thermal Characteristics for the AX58101

Symbol	Description	Condition	Min	Typ	Max	Unit
Θ_{JC}	Thermal resistance of junction to case		-	16	-	°C/W
Θ_{JA}	Thermal resistance of junction to ambient	Still air	-	28.9	-	°C/W
Ψ_{JT}	Junction to Top of the Package Characterization Parameter		-	1.9	-	°C/W

Table 4-6: Thermal Characteristics for the AX58102

Symbol	Description	Condition	Min	Typ	Max	Unit
Θ_{JC}	Thermal resistance of junction to case		-	16	-	°C/W
Θ_{JA}	Thermal resistance of junction to ambient	Still air	-	27.5	-	°C/W
Ψ_{JT}	Junction to Top of the Package Characterization Parameter		-	2.0	-	°C/W

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4.3 Power-On-Reset (POR) Specification

Below figures and table show the two POR circuit spec during power ramp-up/down, and internal behavior the VCCK and the VCC3IO is “wire and“.

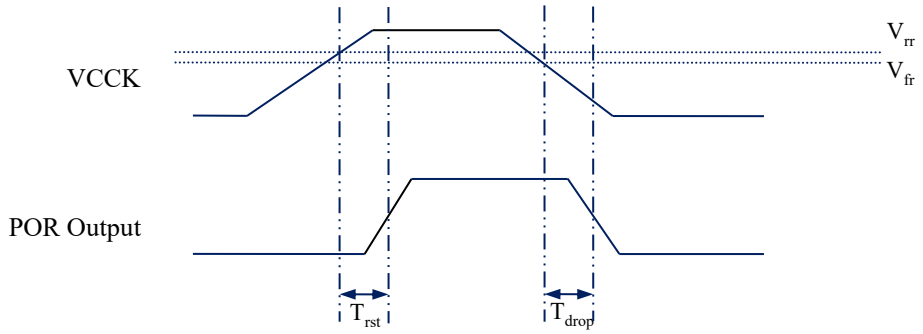

Figure 4-1: Power On Reset (POR) Timing Diagram

Table 4-7: Power On Reset (POR) for the VCCK Timing Table

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
VCCK	Power supply voltage to be detected	-	1.0	1.2	1.32	V
V_{rr}	VCCK rise relax voltage	-	-	0.72	0.9	V
V_{fr}	VCCK fall release voltage	-	-	0.63	0.85	V
T_{rst}	Reset time after POR trigger up, at 1/2*VCCK	VCCK slew rate = 1.0V / 1µs	1.8	2.5	4.8	µs
T_{drop}	Drop time of VCCK to reset, at 1/2*VCCK	VCCK slew rate = 2.5V / 1µs	0.2	0.4	0.9	µs

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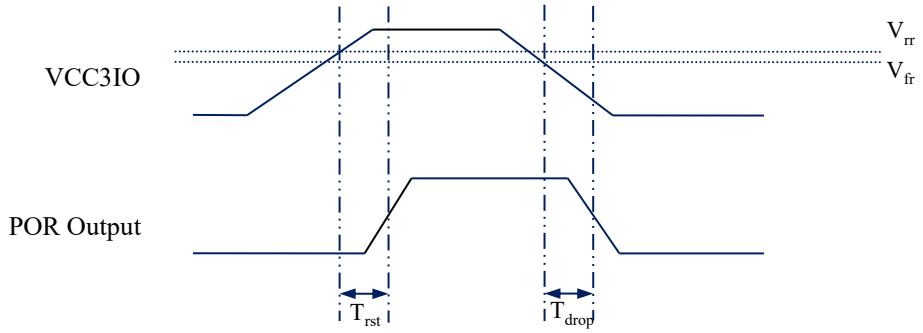

Figure 4-2: Power On Reset (POR) Timing Diagram

Table 4-8: Power On Reset (POR) for the VCC3IO Timing Table

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
VCC3IO	Power supply voltage to be detected	-	2.97	3.3	3.63	V
V_{rr}	VCC3IO rise relax voltage	-	1.9	2.2	2.65	V
V_{fr}	VCC3IO fall release voltage	-	1.6	2.0	2.4	V
T_{rst}	Reset time after POR trigger up, at 1/2* VCC3IO	VCC3IO slew rate = 0.01V / µs	2.02	2.52	3.30	µs
T_{drop}	Drop time of VCC3IO to reset, at 1/2* V_{fr}	VCC3IO slew rate = 1 V/µs	4.21	5.34	6.29	µs

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4.4 Power–up Sequence

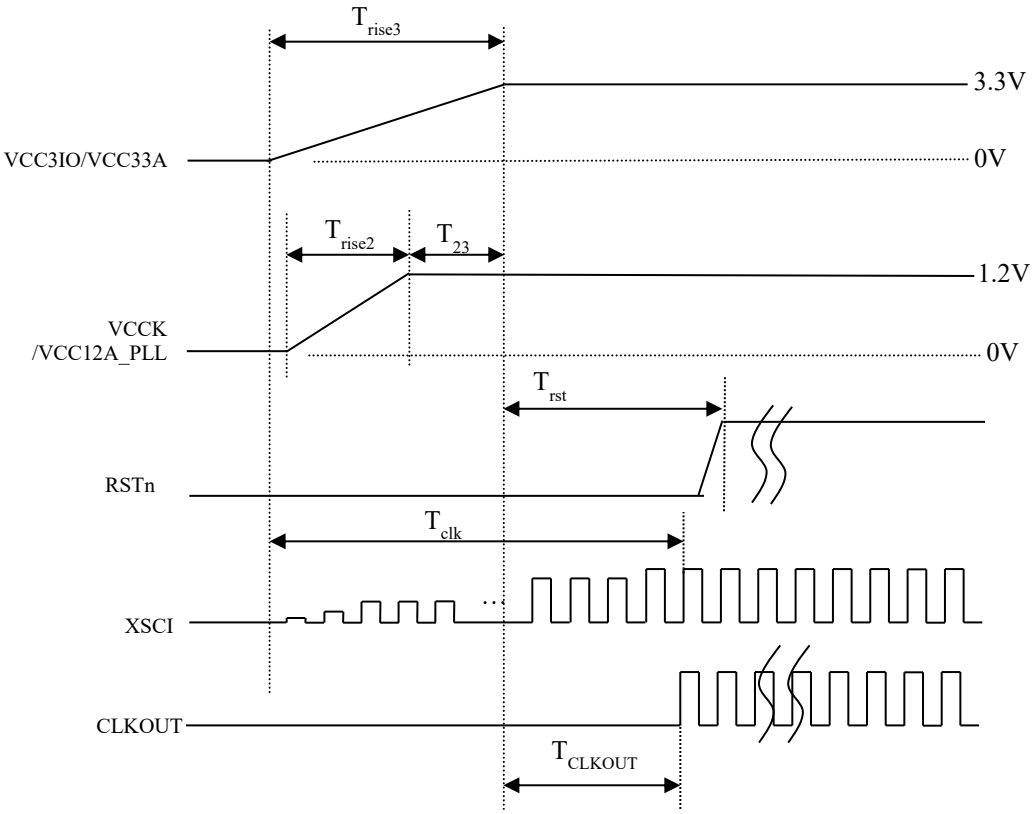

Figure 4-3: Power-up Sequence Timing Diagram

Table 4-9: Power-up Sequence Timing Table

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{rise3}	3.3V power supply rise time	From 0V to 3.3V.	-	600	-	us
T_{rise2}	1.2V power supply rise time	From 0V to 1.2V.	-	200	-	us
T_{23}	VCCK rising to 1.2V to VCC3IO rising to 3.3V interval		-	400	-	us
T_{rst}	RSTn asserted low level interval	From VCC3IO rising to 3.3V to RSTn going high.	40	-	-	us
T_{clk}	25MHz crystal oscillator start-up time	From VCC3IO rising to 3.3V to clock stable of 25MHz crystal oscillator	-	9.2	-	ms
T_{CLKOUT}	CLKOUT output time	Only for the CLKOUT enable	-	8.8	-	ms

Note 1: The above typical timing data is measured from AX58101(2) test board.
Note 2: The VCC33A includes VCC33A_XTAL, VCC33A_PHY0 and VCC33A_PHY1, the VCC12A includes VCC12A_PLL, VCC12A_PHY0 and VCC12A_PHY1.
Note 3: T_{rst} = PLL stable(30us) + XTAL_PAD (control by VCCK)

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4.4.1 Situation for the VCCK started before than the VCC3IO

When VCCK (1.2V) ramps up and exceeds 0.7V, and VCC3IO (3.3V) begins to ramp up, the IOs remain in a tri-state (high impedance, Z) to prevent unintended output. After the 'EEP_DONE' signal goes high and the IOs are configured as outputs, their behavior changes to logic low ('0').

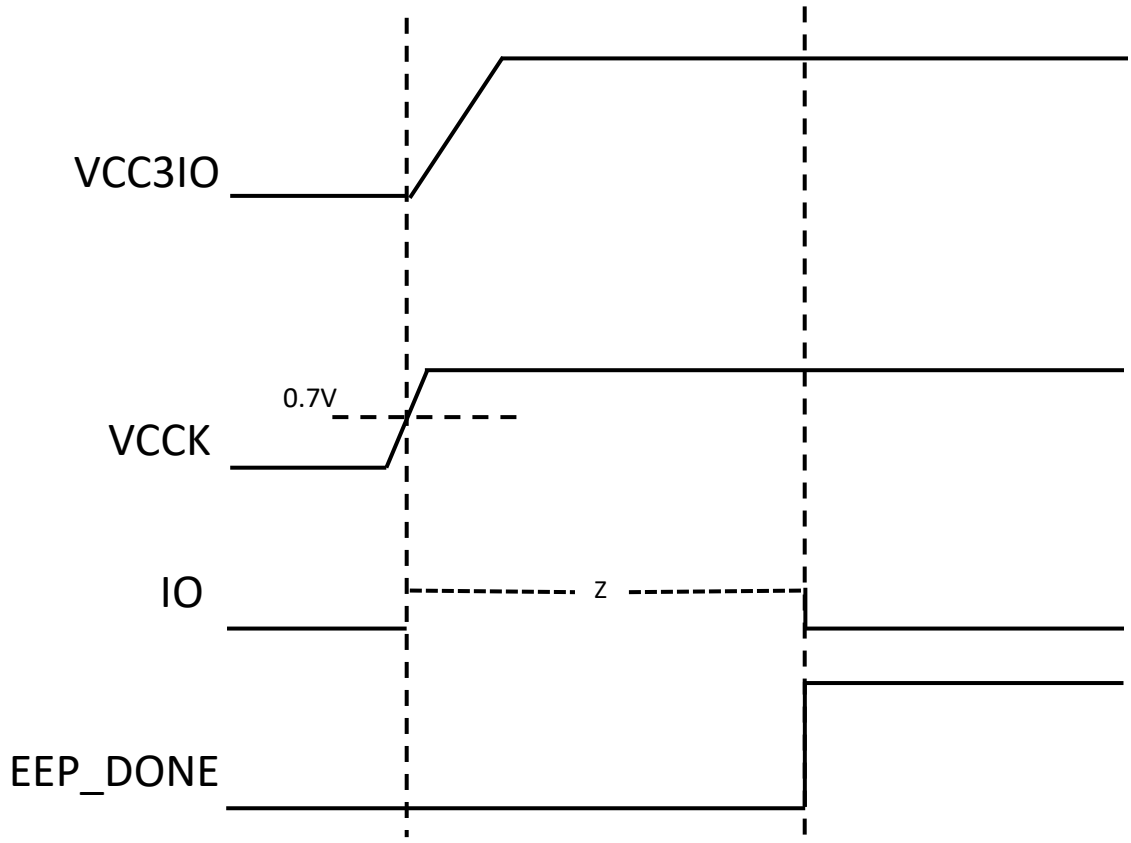

Figure 4-4: Situation for the VCCK started before than the VCC3IO

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4.4.2 Situation for the VCCK and the VCC3IO start as the same time

When VCCK and VCC3IO ramp up simultaneously, the IO initially follows the VCC3IO ramp-up. Once VCCK reaches 0.7V, the IO transitions to a tri-state (Z). After the “EEP_DONE” pin goes high, and the IOs are configured as outputs their behavior changes to logic low ('0').

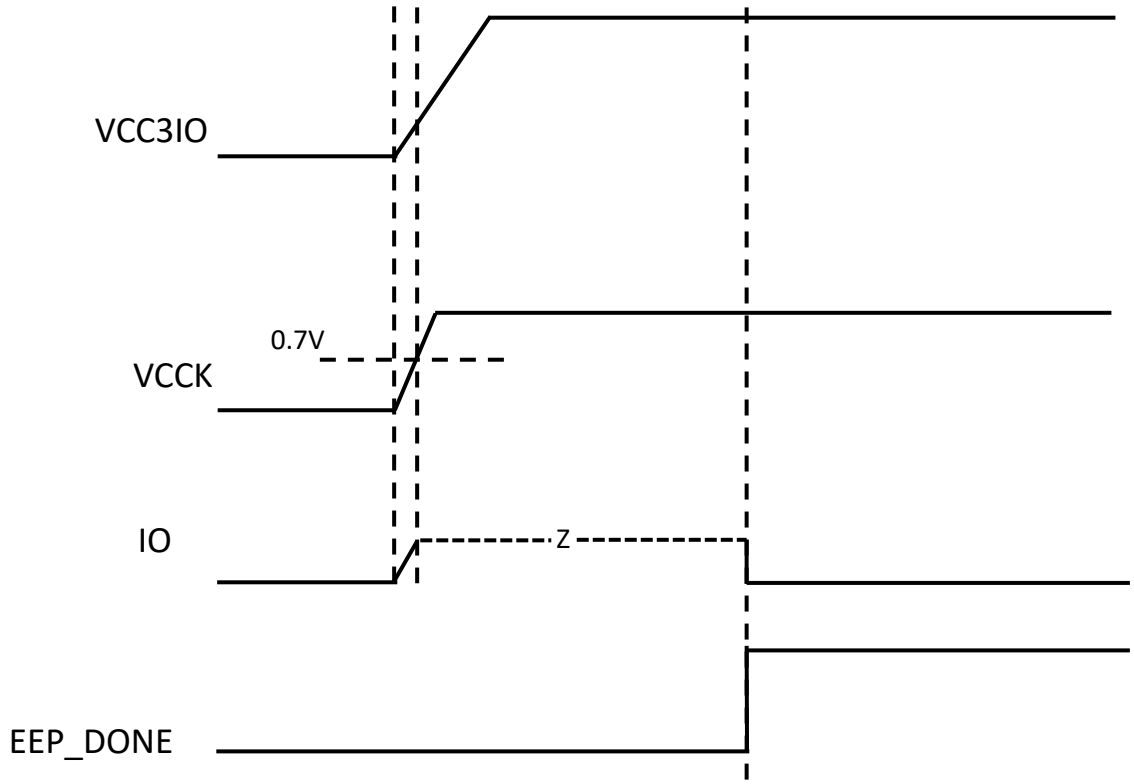

Figure 4-5: Situation for the VCCK and the VCC3IO start as the same time

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4.5 AC Timing Characteristics

4.5.1 I²C Timing

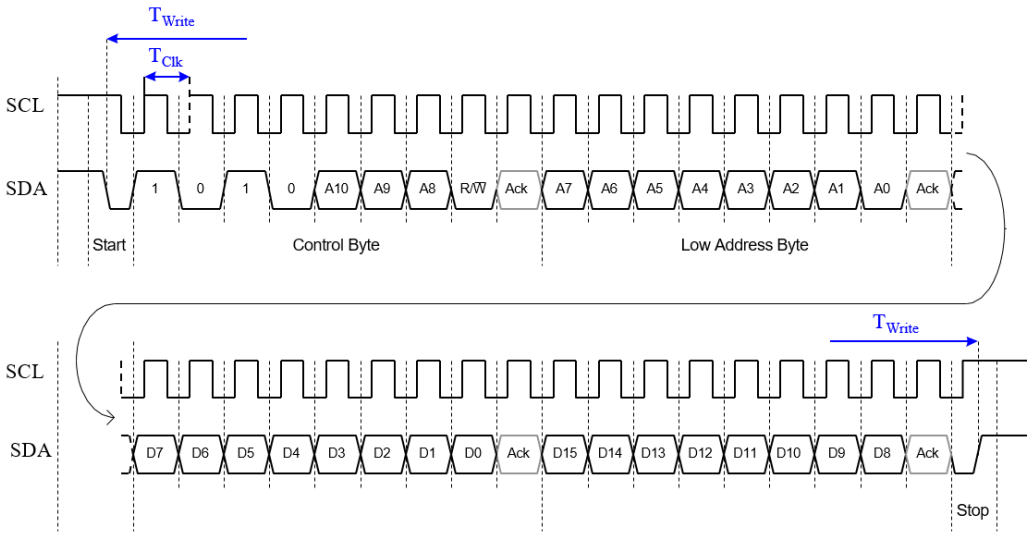

Figure 4-6: Write access (1 address byte, up to 16 Kbit EEPROMs)

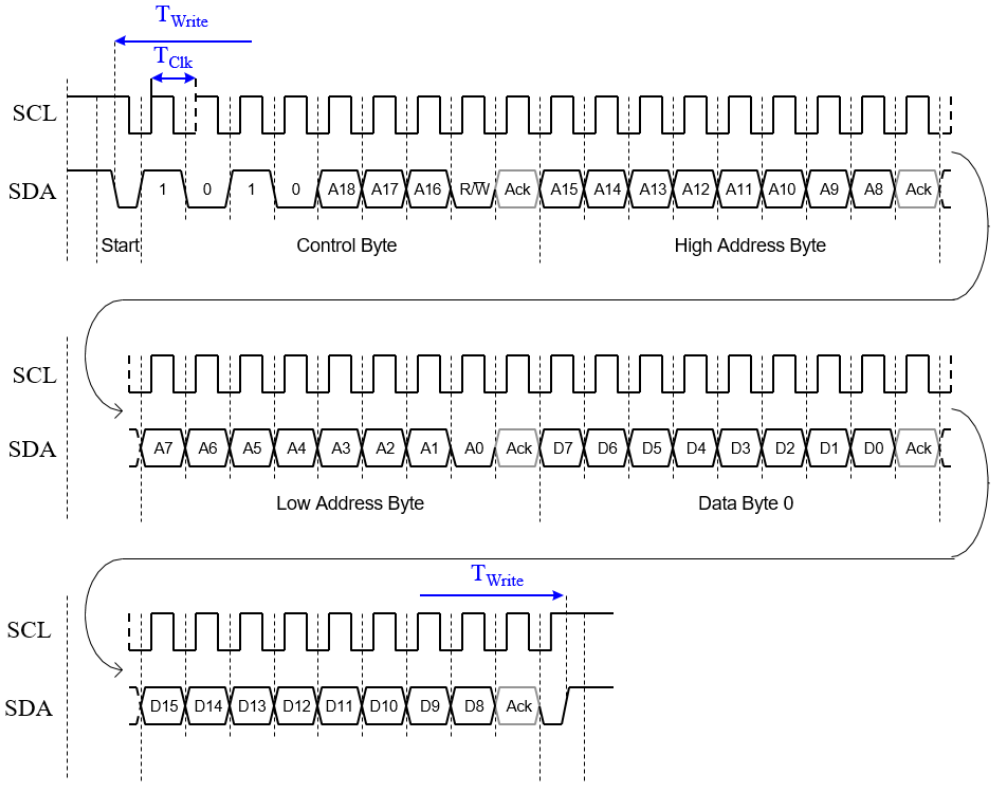

Figure 4-7: Write access (2 address bytes, 32 Kbit - 4 Mbit EEPROMs)

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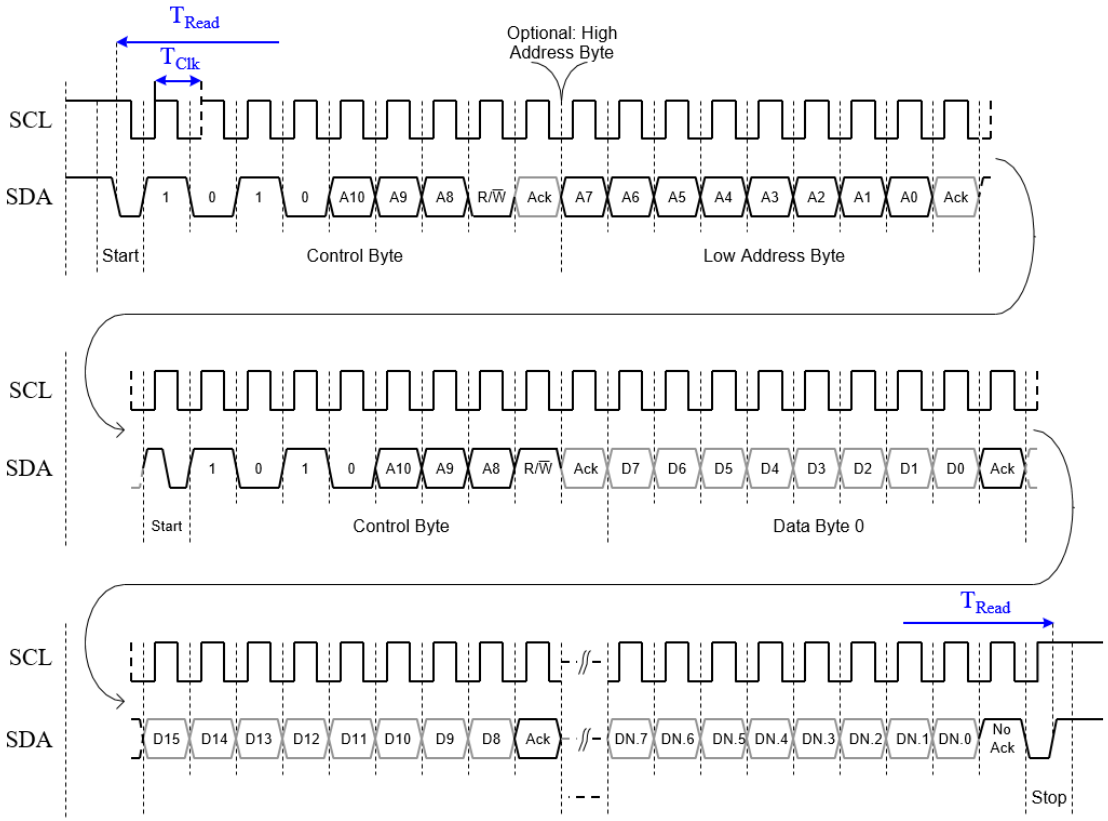

Figure 4-8: Read access (1 address byte, up to 16 Kbit EEPROMs)

Table 4-10: I²C EEPROM Timing Table

Symbol	Parameter		Typical		Units
			Up to 16 Kbit	32 Kbit-4 Mbit	
T_{Clk}	EEPROM clock period		6.72 (≈ 150 KHz)		us
T_{Write}	Write access time (without errors)		250	310	us
T_{Read}	Read access time (without errors):	2 words	440	500	us
		configuration (8 Words)	1.16	1.22	ms
T_{Delay}	Time until configuration loading begins after Reset is gone		65.5		us

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4.5.2 Port 2/3 MII Timing

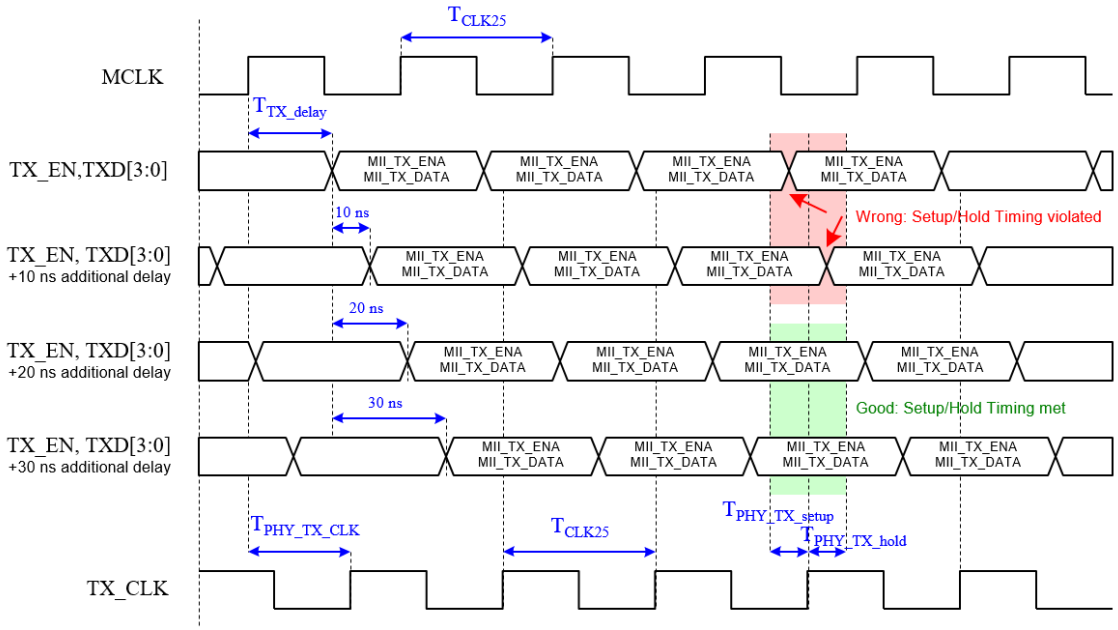

Figure 4-9: Port 2/3 MII TX Timing Diagram

Table 4-11: Port 2/3 MII TX Timing Table

Symbol	Description	Min	Typ	Max	Units
T_{CLK25}	MCLK output	-	40	-	ns
T_{TX_delay}	TX_EN/TXD[3:0] delay after rising edge of MCLK	-	-	2	ns
$T_{PHY_TX_CLK}$	Delay between MCLK and TX_CLK output of the PHY	-	PHY dependent	-	ns
$T_{PHY_TX_setup}$	PHY setup time	PHY dependent	-	-	ns
$T_{PHY_TX_hold}$	PHY hold time	PHY dependent	-	-	ns

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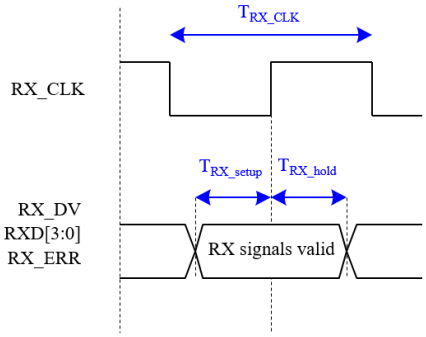

Figure 4-10: Port 2/3 MII RX Timing Diagram

Table 4-12: Port 2/3 MII RX Timing Table

Symbol	Description	Min	Typ	Max	Units
T_{RX_CLK}	RX_CLK period (100 PPM with maximum FIFO Size only)	-	40	-	ns
T_{RX_setup}	RX_DV/RX_ER/RXD[3:0] valid before rising edge of RX_CLK	2.1	-	-	ns
T_{RX_hold}	RX_DV/RX_ER/RXD[3:0] valid after rising edge of RX_CLK	0.5	-	-	ns

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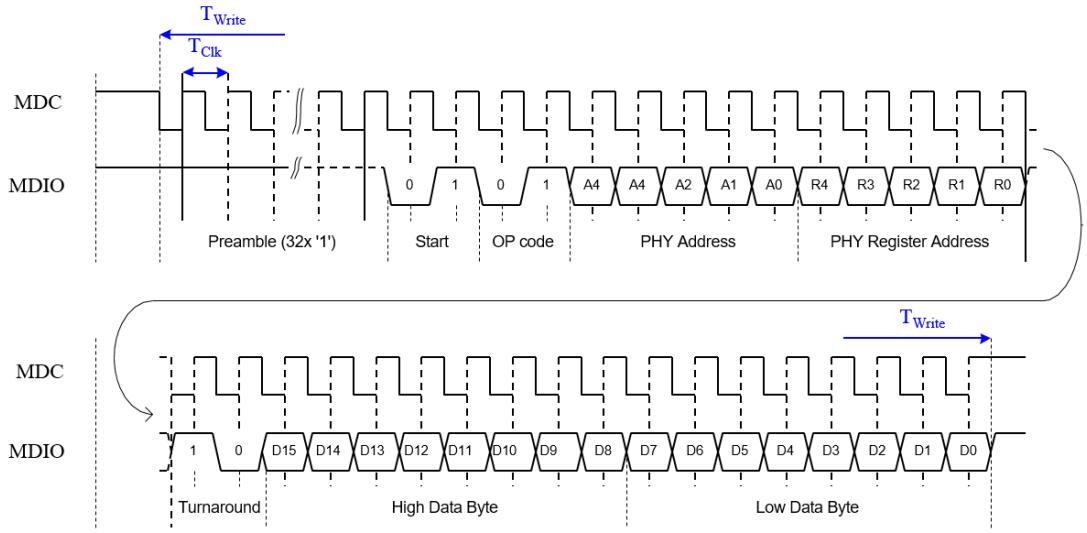

Figure 4-11: MDC/MDIO Write access

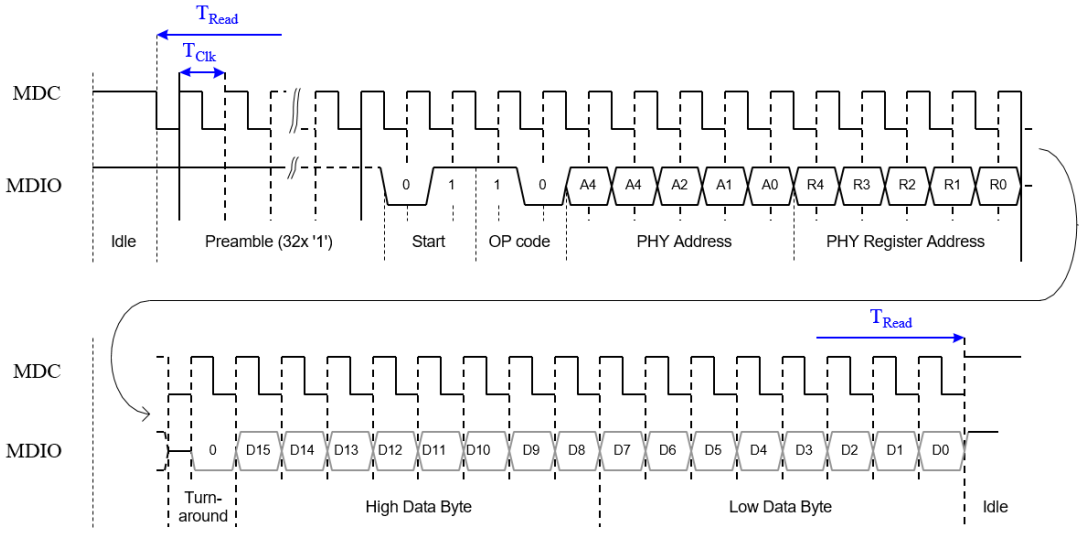

Figure 4-12: MDC/MDIO Read access

Table 4-13: MDC/MDIO Timing Table

Symbol	Description	Min	Typ	Max	Units
T_{MDC}	MDC period		400 (≈ 2.5 MHz)		ns
T_{Write}	MI Write access time		25.6		us
T_{Read}	MI Read access time		25.4		us
$T_{MI_startup}$	Time between reset end and the first access of MI Link detection and configuration		1.34		ms

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4.5.3 Distributed Clocks SYNC/LATCH

Table 4-14: DC SYNC/LATCH timing characteristics

Symbol	Description	Min	Typ	Max	Units
T_{DC_LATCH}	Time between LATCH 0/1 events	12			ns
$T_{DC_SYNC_Jitter}$	SYNC 0/1 output jitter			12	ns

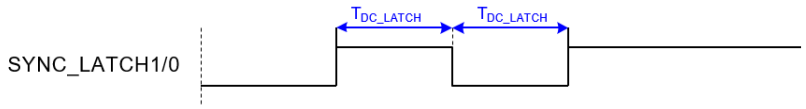

Figure 4-13: LATCH timing

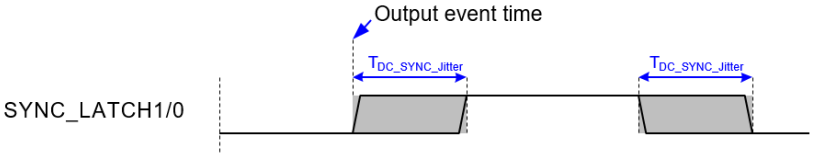

Figure 4-14: SYNC timing

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4.5.4 Digital I/O Timing

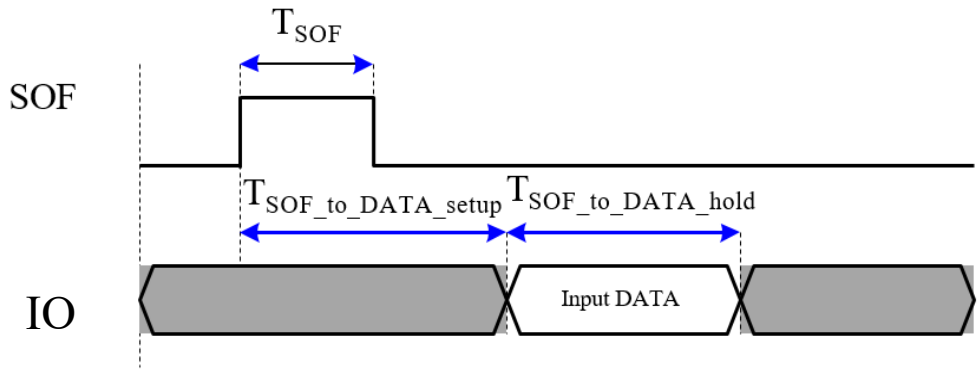

Figure 4-15: Digital Input: Input data sampled at SOF, IO can be read in the same frame

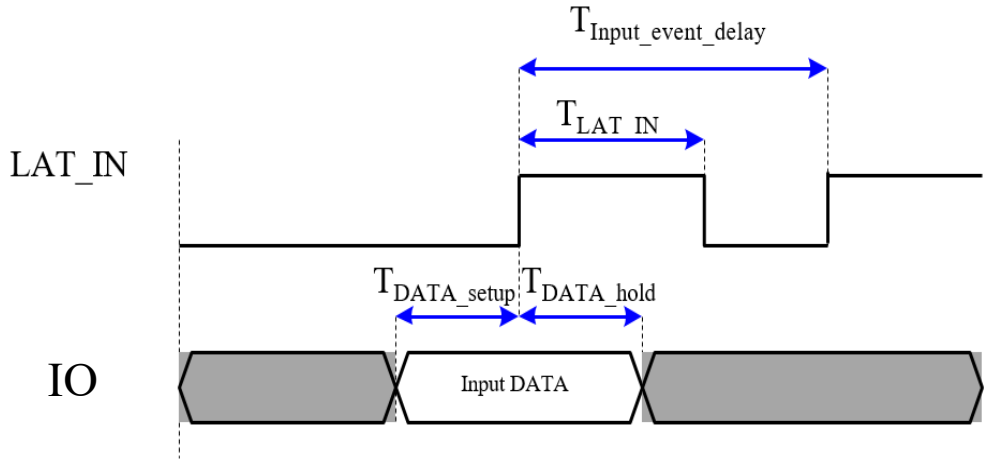

Figure 4-16: Digital Input: Input data sampled with LATCH_IN

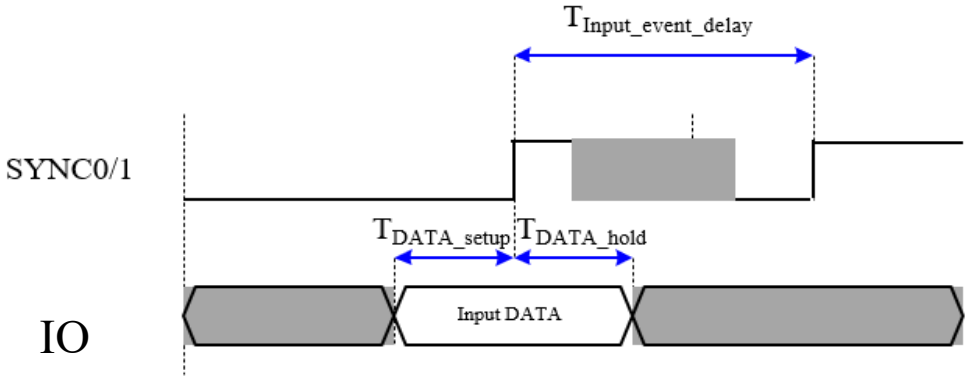

Figure 4-17: Digital Input: Input data sampled with SYNC0/1

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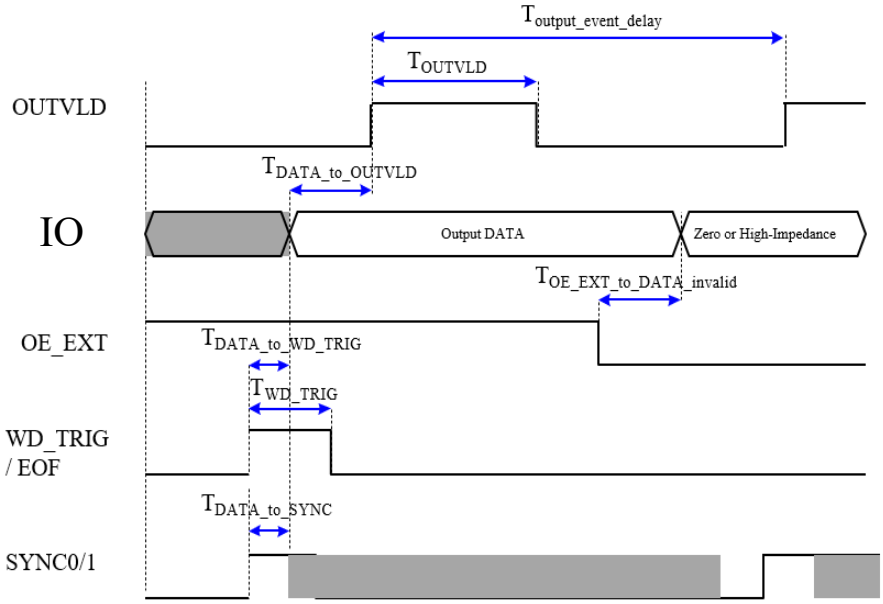

Figure 4-18: Digital Output timing

Table 4-15: Digital I/O timing Table

Symbol	Description	Min	Typ	Max	Units
T_{DATA_setup}	Input data valid before LAT_IN	5	-	-	ns
T_{DATA_hold}	Input data valid after LAT_IN	2	-	-	ns
T_{LAT_IN}	LAT_IN high time	4	-	-	ns
T_{SOF}	SOF high time	-	40	-	ns
$T_{SOF_to_DATA_setup}$	Input data valid after SOF, so that Inputs can be read in the same frame	0	-	1.2	us
$T_{SOF_to_DATA_hold}$	Input data invalid after SOF	1.6	-	-	us
$T_{input_event_delay}$	Time between consecutive input events	440	-	-	ns
T_{OUTVLD}	OUTVLD high time	-	80	-	ns
$T_{DATA_to_OUTVLD}$	Output data valid before OUTVLD	79	-	-	ns
T_{WD_TRIG}	WD_TRIG high time	-	40	-	ns
$T_{DATA_to_WD_TRIG}$	Output data valid after WD_TRIG	-	-	20	ns
$T_{DATA_to_EOF}$	Output data valid after EOF	-	-	20	ns
$T_{DATA_to_SYNC}$	Output data valid after SYNC0/1	-	-	20	ns
$T_{OE_EXT_to_DATA_invalid}$	Outputs zero or Outputs hi-Z after OE_EXT set to low	0	-	9.5	ns
$T_{output_event_delay}$	Time between consecutive output events	320	-	-	ns
$T_{OUT_EXT_valid}$	OUT_EXT valid before OUTVLD	-	80	-	ns
$T_{OUT_EXT_invalid}$	OUT_EXT invalid after OUTVLD	-	80	-	ns

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4.5.5 ESC PDI SPI Slave Timing

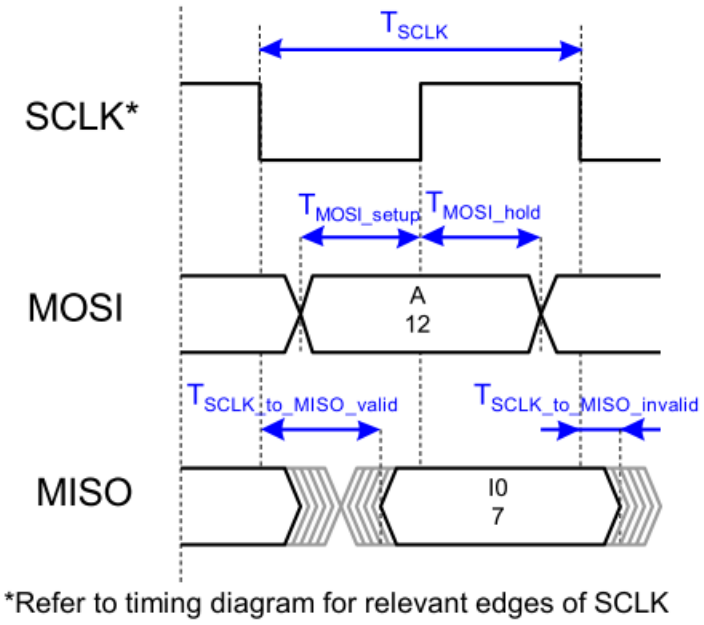

Figure 4-19: Basic MOSI/MISO timing

Table 4-16: PDI SPI Slave Timing Table

Symbol	Description		Min	Typ	Max	Units
T_{SCLK}	SCLK period		33 (≤30MHz)	-	-	ns
$T_{SEL_to_CLK}$	First SCLK cycle after SCS_ESC asserted		5	-	-	ns
$T_{CLK_to_SEL}$	Deassertion of SCS_ESC after last SCLK cycle	SPI mode 0/2, SPI mode 1/3 with normal data out sample	5	-	-	ns
		SPI mode 1/3 with late data out sample	T_{CLK}/2+ 5			
T_{read}	Only for read access between address/command and first data byte. Can be ignored if BUSY or Wait State Bytes are used.		240	-	-	ns
T_{access_delay}	Delay between SPI accesses		40	-	-	ns
T_{MOSI_setup}	MOSI valid before SCLK edge		3	-	-	ns
T_{MOSI_hold}	MOSI valid after SCLK edge		0	-	-	ns
$T_{SCLK_to_MISO_valid}$	MISO valid after SCLK edge		-	-	10.5	ns
$T_{SCLK_to_MISO_invalid}$	MISO invalid after SCLK edge		0	-	-	ns
T_{IRQ_delay}	Internal delay between AL event and SINT output to enable correct reading of the interrupt registers.		-	180	-	ns

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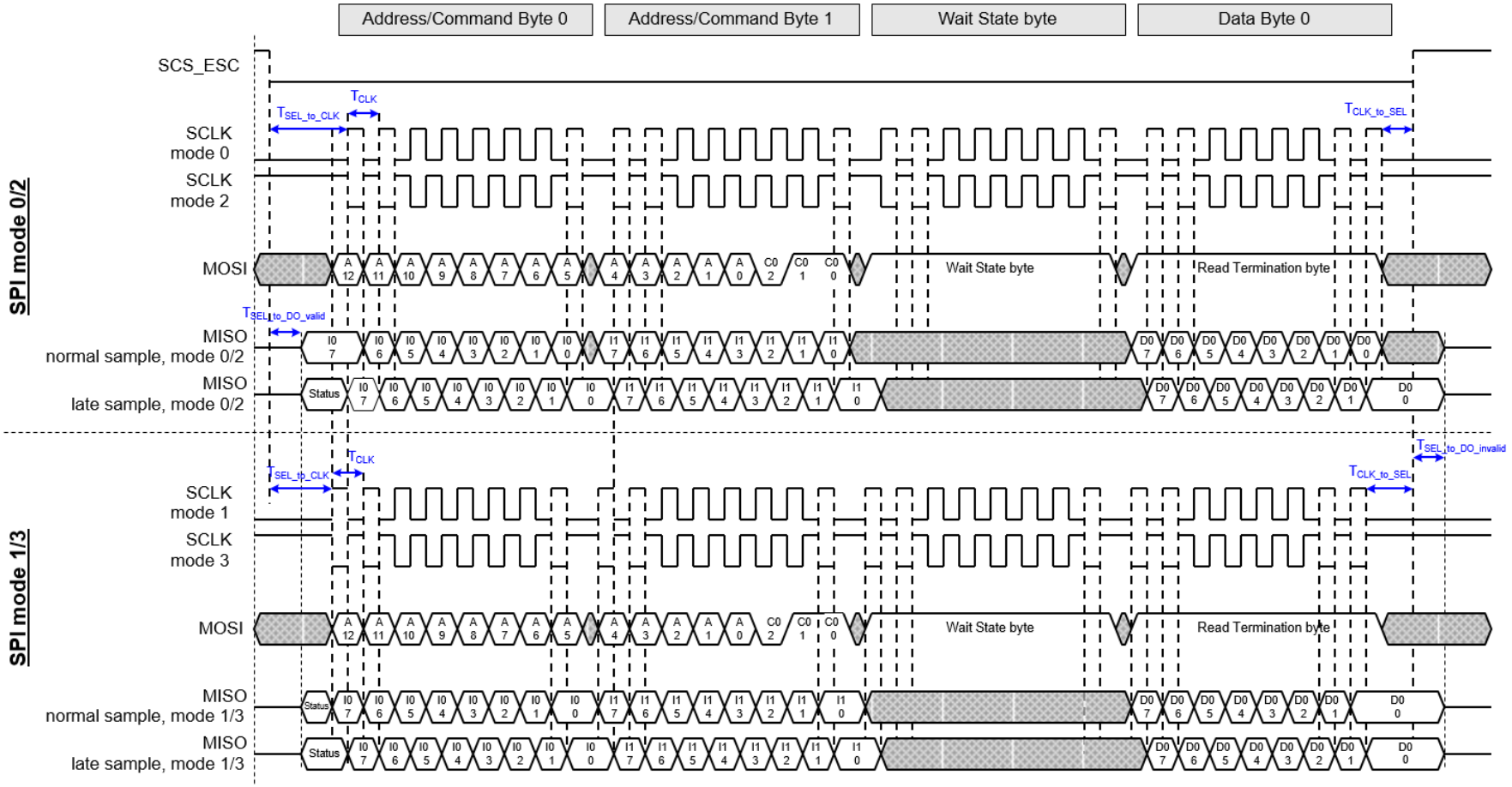

Figure 4-20: PDI SPI Slave read access (2 byte addressing, 1 byte read data) with Wait State byte

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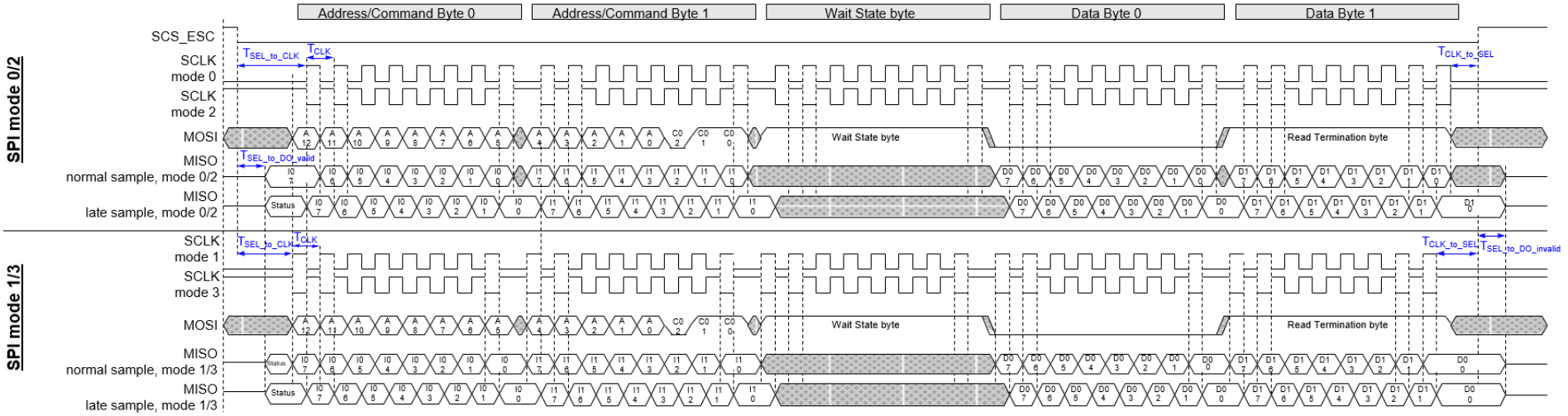

Figure 4-21: PDI SPI Slave read access (2 byte addressing, 2 byte read data) with Wait State byte

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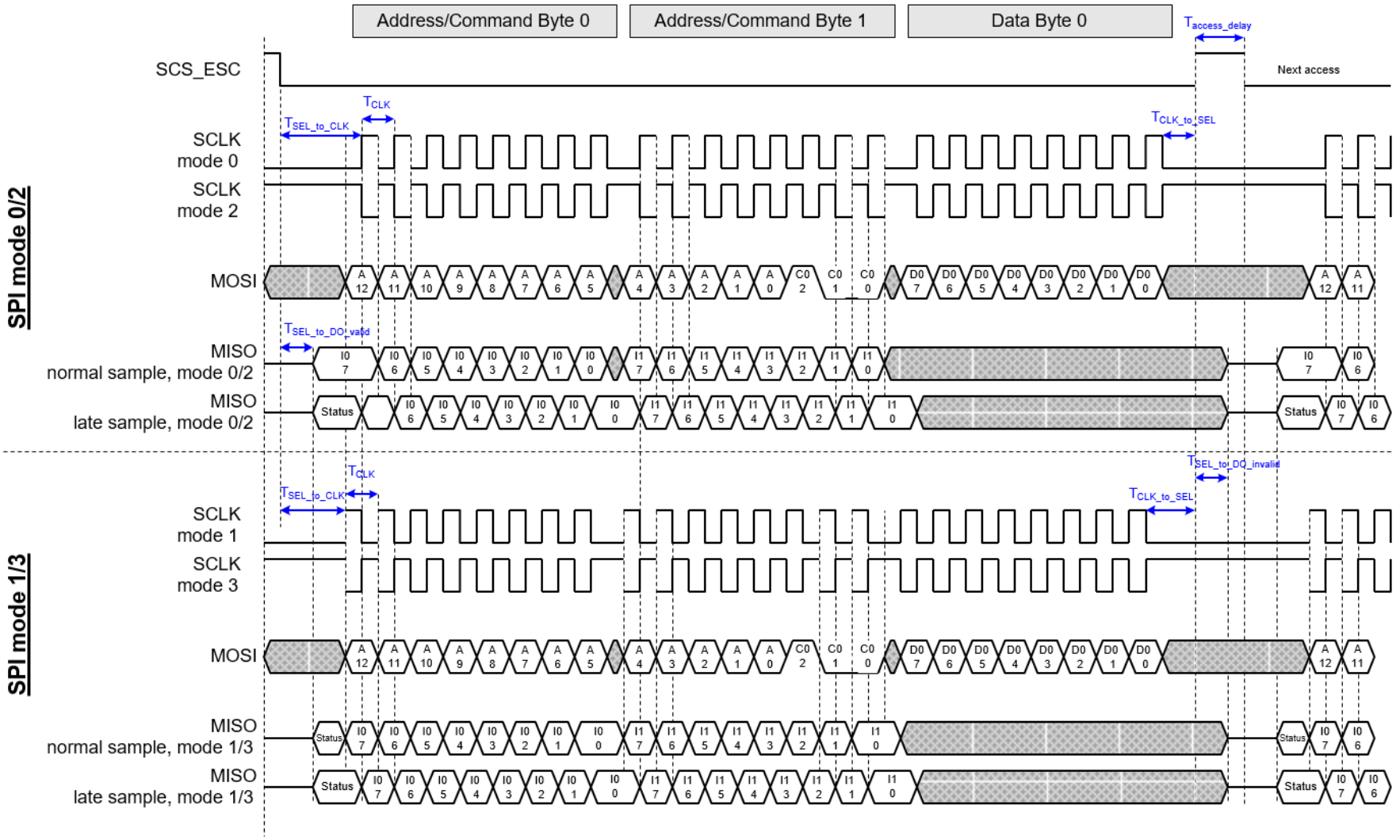

Figure 4-22: PDI SPI Slave write access (2 byte addressing, 1 byte write data)

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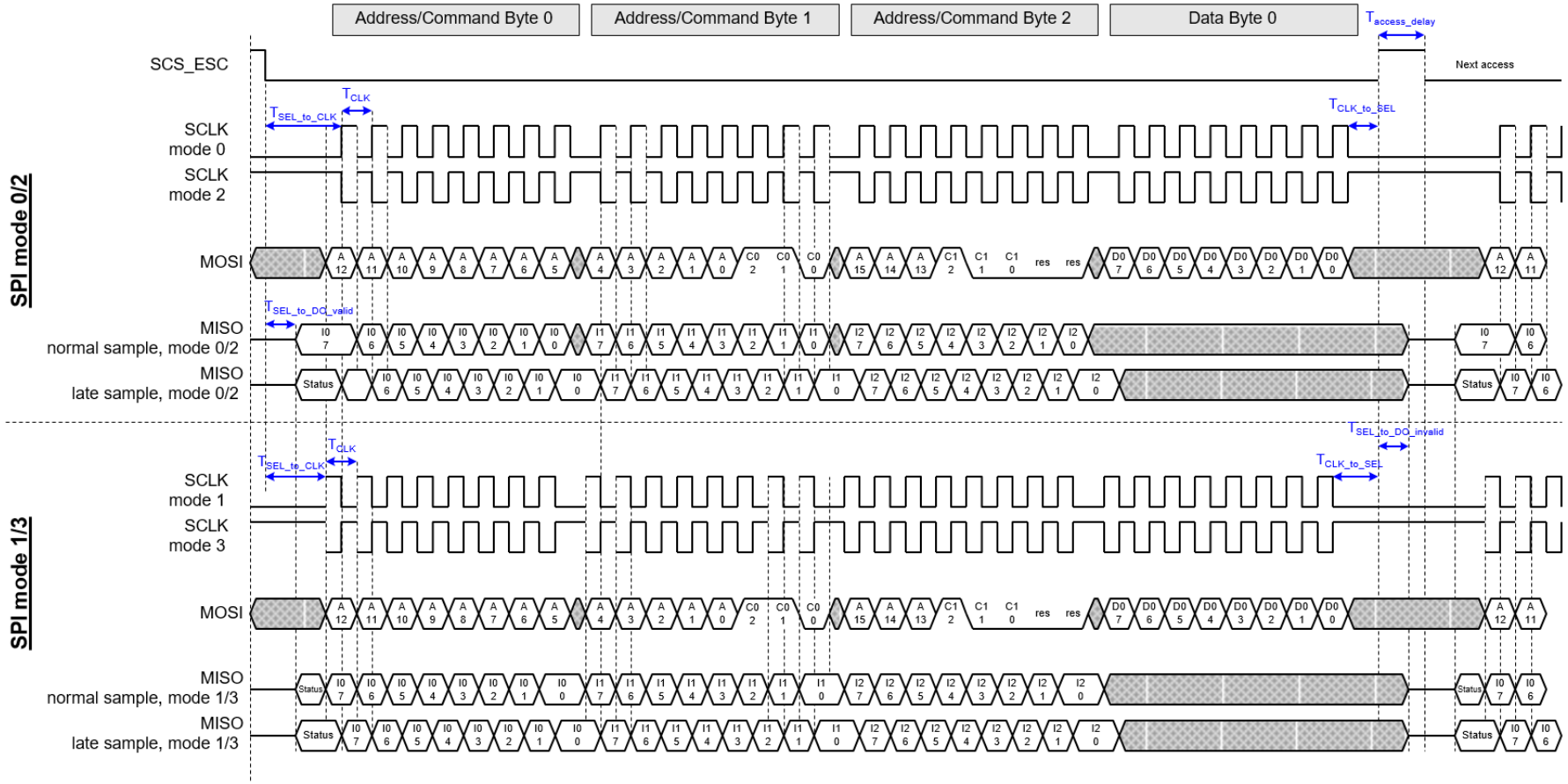

Figure 4-23: PDI SPI Slave write access (3 byte addressing, 1 byte write data)

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4.5.6 Function SPI Slave Timing

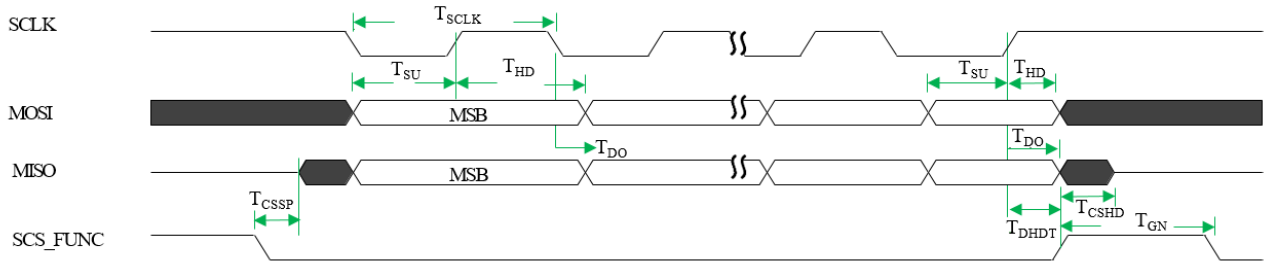

Figure 4-24: Function SPI Slave with share pin Timing Diagram

Table 4-17: Function SPI with share pin Timing Table

Symbol	Description	Min	Typ	Max	Units
T_{SCLK}	SCLK clock period	-	-	47	MHz
T_{DO}	MISO data valid time after SCLK edge	10.5	-	-	ns
T_{SU}	MOSI data setup time before SCLK edge	2	-	-	ns
T_{HD}	MOSI data hold time after SCLK edge	2	-	-	ns
T_{CSSP}	SCS setup time before MISO active	7.7	-	-	ns
T_{DHD}	SCS hold time after SCLK edge	21	-	-	ns
T_{CSHD}	MISO data hold time after SCS de-assert	2.5	-	-	ns
T_{GN}	SCS negation to next SCS assertion time	40	-	-	ns

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4.5.7 ESC PDI Local Bus Timing

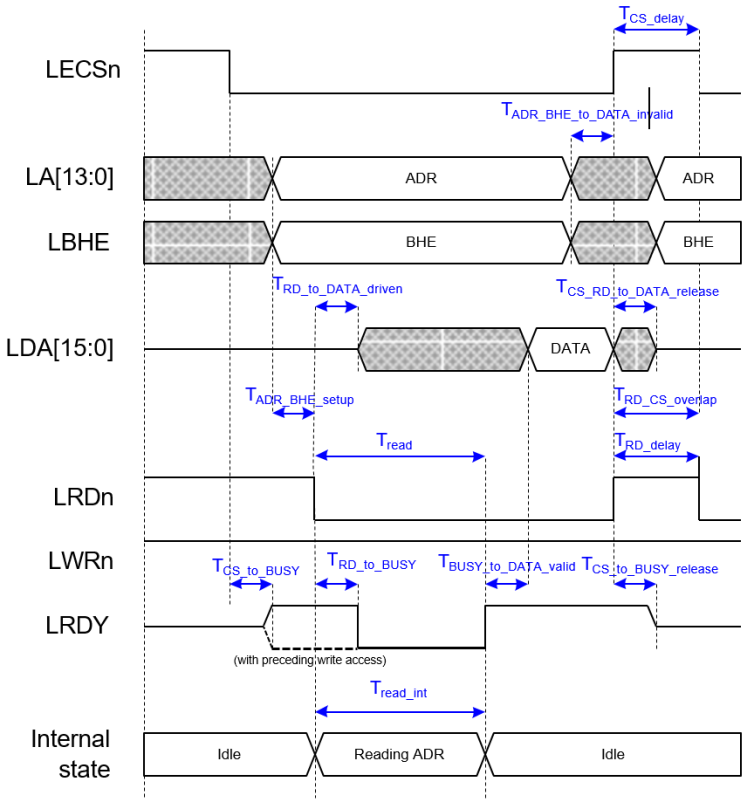

Figure 4-25: PDI Local Bus Read access (without preceding write access)

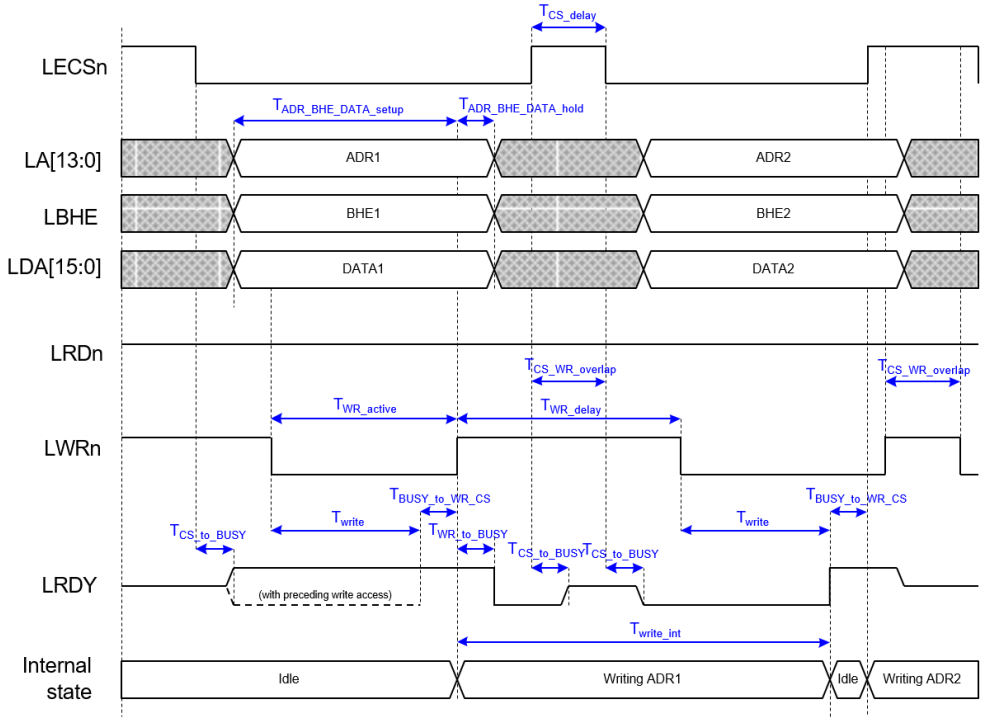

Figure 4-26: PDI Local Bus Write access (write after rising edge LWRn, without preceding write access)

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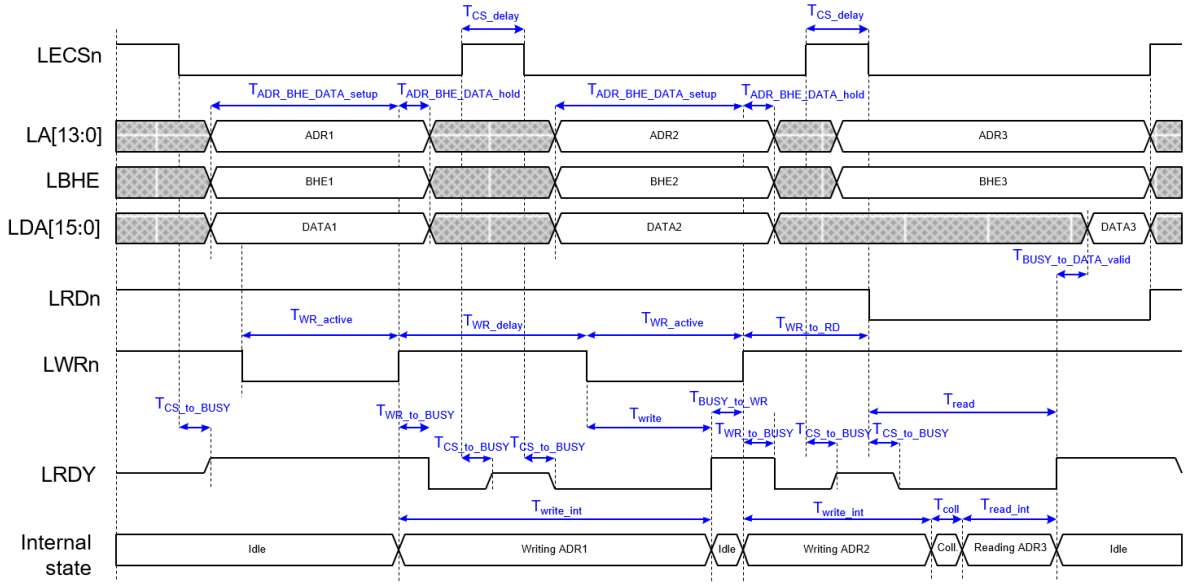

Figure 4-27: PDI Local Bus Sequence of two write accesses and a read access

Note: The first write access to ADR1 is performed after the first rising edge of WR. After that, the ESC is internally busy writing to ADR1. After CS is deasserted, BUSY is not driven any more, nevertheless, the ESC is still writing to ADR1.

Hence, the second write access to ADR2 is delayed because the write access to ADR1 has to be completed first. So, the second rising edge of WR must not occur before BUSY is gone. After the second rising edge of WR, the ESC is busy writing to ADR2. This is reflected with the BUSY signal as long as CS is asserted.

The third access in this example is a read access. The ESC is still busy writing to ADR2 while the falling edge of RD occurs. In this case, the write access to ADR2 is finished first, and afterwards, the read access to ADR3 is performed. The ESC signals BUSY during both write and read access

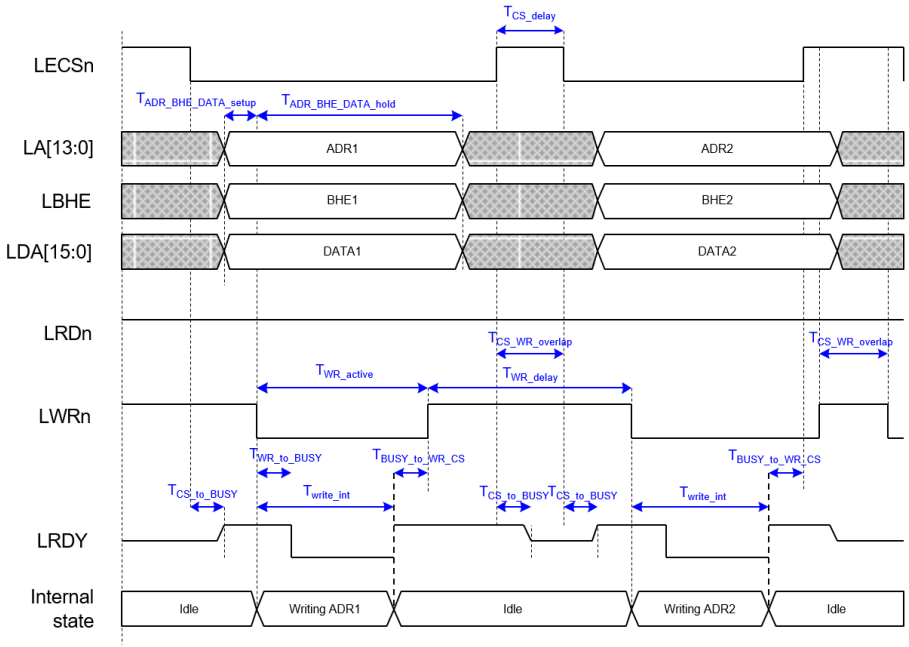

Figure 4-28: PDI Local Bus Write access (write after falling edge LWRn

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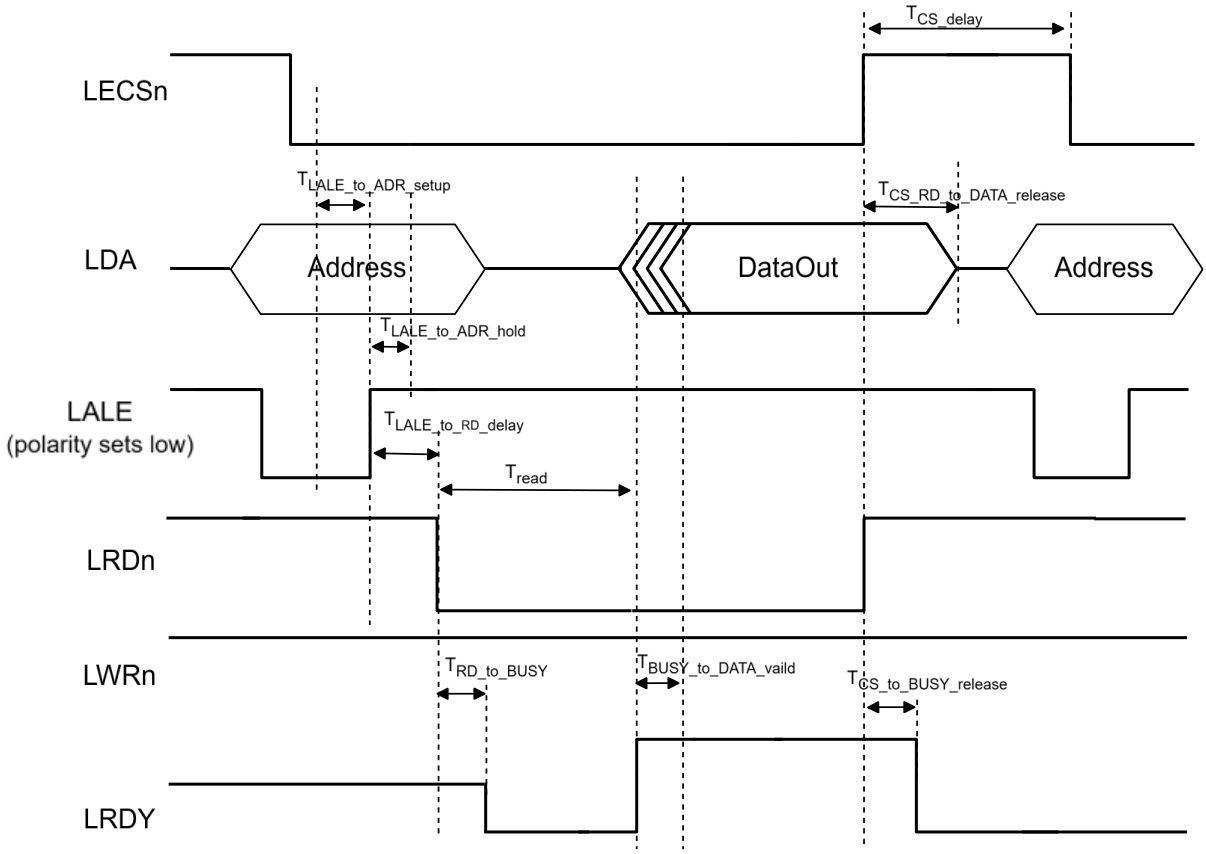

Figure 4-29: PDI Local Bus Read access with AD merge mode (without preceding write access)

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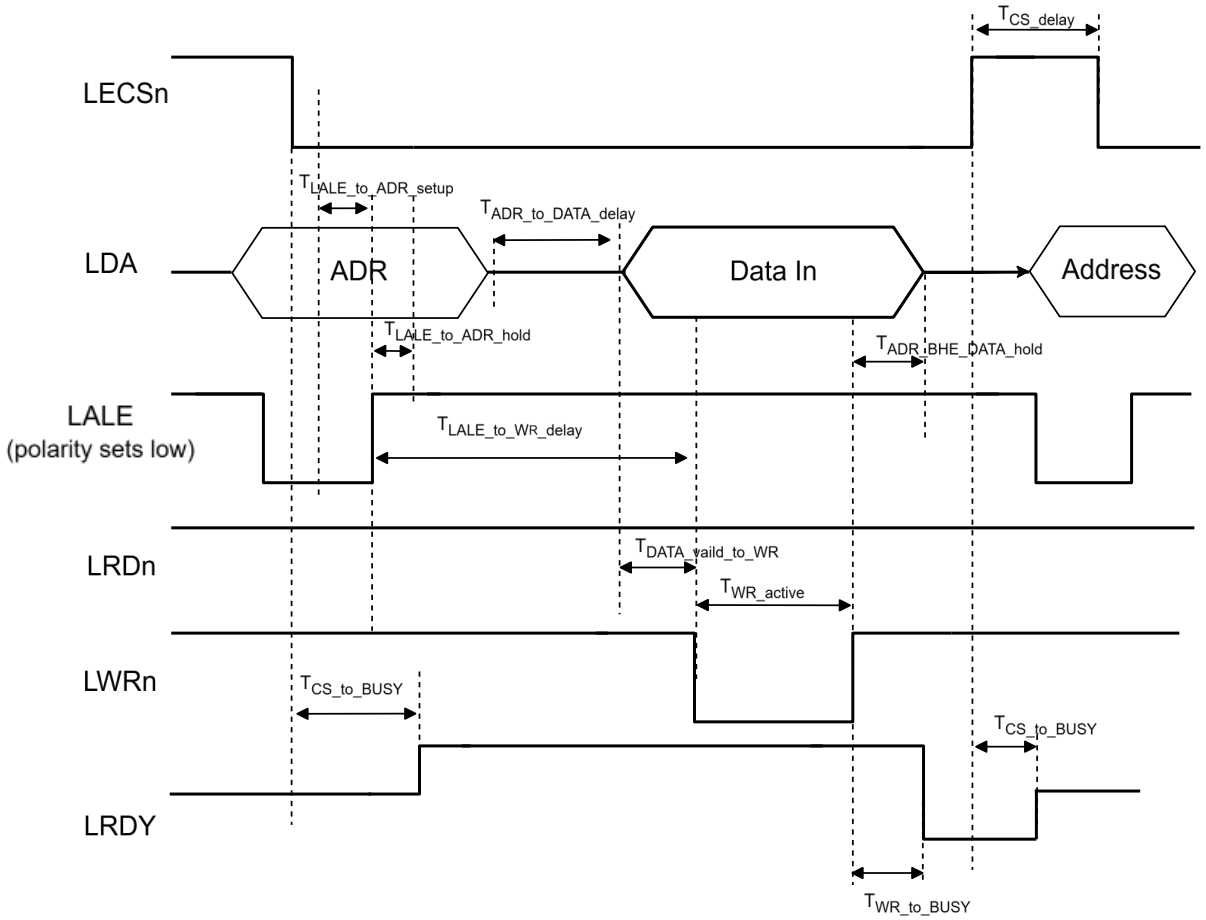

Figure 4-30: PDI Local Bus Write access with AD merge mode (write after rising edge LWRn, without preceding write access)

Table 4-18: PDI Local Bus Timing Table

Symbol	Description	Min	Typ	Max	Units
$T_{CS_to_BUSY}$	BUSY driven and valid after CS assertion	-	-	45	ns
$T_{ADR_BHE_setup}$	ADR and BHE valid before RD assertion	0	-	-	ns
$T_{RD\ to\ DATA\ driven}$	DATA bus driven after RD assertion	0	-	-	ns
$T_{RD\ to\ BUSY}$	BUSY asserted after RD assertion	0	-	10	ns
$T_{LALE\ to\ ADR\ setup}$	LALE latch ADR setup time	2.5	-	-	ns
$T_{LALE\ to\ ADR\ hold}$	LALE latch ADR hold time	2.5	-	-	ns
$T_{LALE_to_RD_delay}$	Delay between LALE deassertion and RD assertion	8	-	-	ns
T_{read}	External read time (RD assertion to BUSY deassertion) with normal read busy output (0x0152[0]). Additional 20 ns if delayed read busy output is configured.				ns
	without preceding write access or $T_{WR_to_RD} \geq T_{prec_write} + T_{Coll}$ or configuration: write after falling edge of WR	-	-	T_{read_int}	
	with preceding write access and $T_{WR_to_RD} < T_{prec_write} + T_{Coll}$	-	-	$T_{read_int} + T_{prec_write} + T_{Coll} - T_{WR\ to\ RD}$	

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	8-bit access, absolute worst case with preceding write access ($T_{WR_to_RD}$=min, T_{prec_write} =max, T_{Coll}=max)		-	-	420	
	16-bit access, absolute worst case with preceding write access ($T_{WR_to_RD}$=min, T_{prec_write} =max, T_{Coll}=max)		-	-	560	
T_{read_int}	Internal read time	8-bit access	-	-	220	ns
		16-bit access			300	
T_{prec_write}	Time for preceding write access	8-bit access	-	-	180	ns
		16-bit access			260	
$T_{BUSY_to_DATA_valid}$	DATA bus valid after device BUSY is deasserted	normal read busy output	-	-	5	ns
		delayed read busy output			-15	
$T_{ADR_BHE_to_DATA_invalid}$	DATA invalid after ADR or BHE change		0	-	-	ns
$T_{CS_RD_to_DATA_release}$	DATA bus released after CS deassertion or RD deassertion		2.5	-	7.5	ns
$T_{CS_to_BUSY_release}$	BUSY released after CS deassertion		2.5	-	8.5	ns
T_{CS_delay}	Delay between CS deassertion an assertion		5	-	-	ns
T_{RD_delay}	Delay between RD deassertion and assertion		5	-	-	ns
$T_{ADR_BHE_DATA_setup}$	ADR, BHE and Write DATA valid before WR deassertion		6.5	-	-	ns
$T_{ADR_BHE_DATA_hold}$	ADR, BHE and Write DATA valid after WR deassertion		2	-	-	ns
T_{WR_active}	WR assertion time		8.5	-	-	ns
$T_{ADR_to_DATA_delay}$	In AD merge mode, there is a delay between the ADR and the write data transformers		2	-	-	ns
$T_{LALE_to_WR_delay}$	Delay between LALE deassertion and WR assertion		4	-	-	ns
$T_{DATA_valid_to_WR}$	DATA valid before WR assertion		2	-	-	ns
$T_{BUSY_to_WR_CS}$	WR or CS deassertion after BUSY deassertion		0	-	-	ns
$T_{WR_to_BUSY}$	BUSY assertion after WR deassertion		-	-	12	ns
T_{write}	External write time (WR assertion to BUSY deassertion)					ns
	Configuration: write after falling edge of WR (act. low)		0	-	T_{write_int}	
	with preceding write access and $T_{WR_delay} < T_{write_int}$ (Write after rising edge -of WR)			-	T_{write_int} - T_{WR_delay}	ns
	without preceding write access or $T_{WR_delay} \geq T_{write_int}$ (Write after rising edge of WR)			-	0	
	8-bit access, absolute worst case with preceding write access (T_{WR_delay}= min, T_{WR_int}=max, Write after rising edge of WR)			-	180	
	16-bit access, absolute worst case with preceding write access			-	260	

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	(T_{WR_delay}=min, T_{WR_int}=max, Write after rising edge of WR)					
T_{write_int}	Internal write time	8-bit access	-	-	180	ns
		16-bit access			260	
T_{WR_delay}	Delay between WR deassertion and assertion		5	-	-	ns
T_{Coll}	Extra read delay	RD access directly follows WR access with the same address (8-bit accesses or 8-bit WR and 16-bit RD)	-	-	20	ns
		different addresses or 16-bit accesses			0	
$T_{WR_to_RD}$	Delay between WR deassertion and RD assertion		0	-	-	ns
$T_{CS_WR_overlap}$	Time both CS and WR have to be deasserted simultaneously (only if CS is deasserted at all)		5	-	-	ns
$T_{CS_RD_overlap}$	Time both CS and RD have to be deasserted simultaneously (only if CS is deasserted at all)		5	-	-	ns
T_{IRQ_delay}	Internal delay between AL event and LINT output to enable correct reading of the interrupt registers.		-	180	-	ns

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4.5.8 Function Local Bus Timing

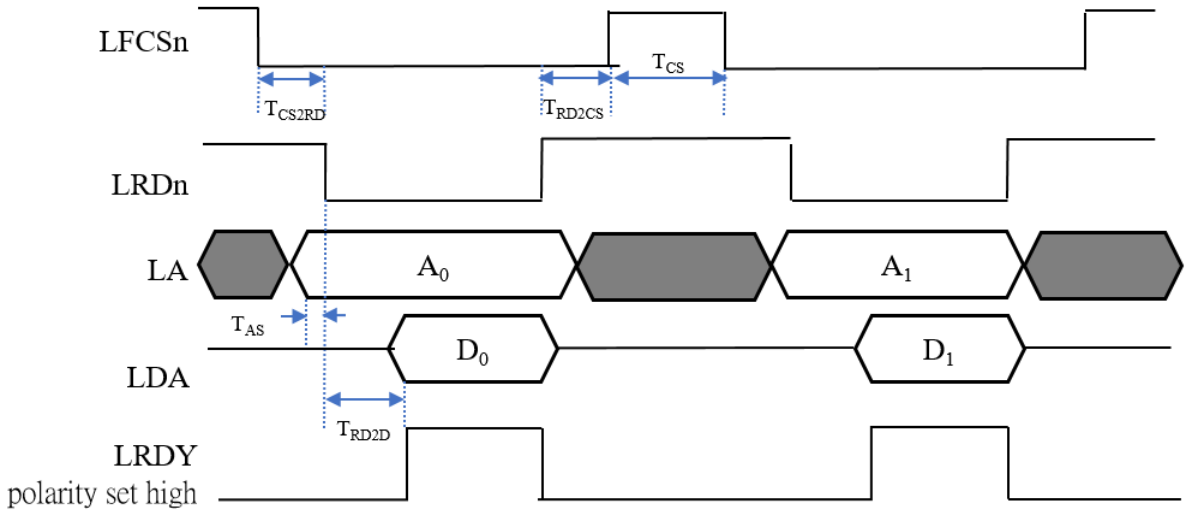

Figure 4-31: Function Local Bus Signal Read Access

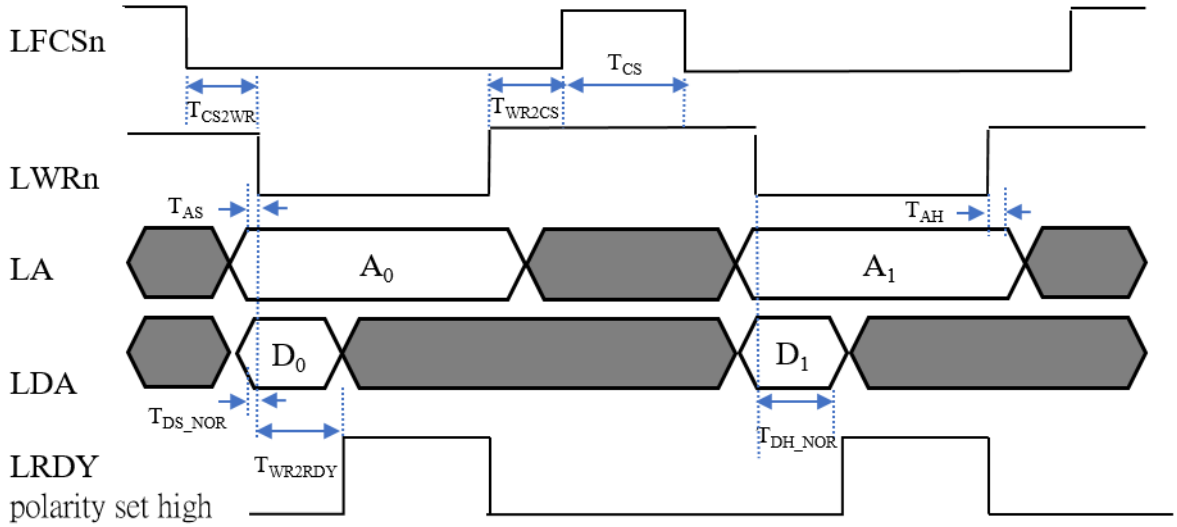

Figure 4-32: Function Local Bus Write Access (Late Sample = 0)

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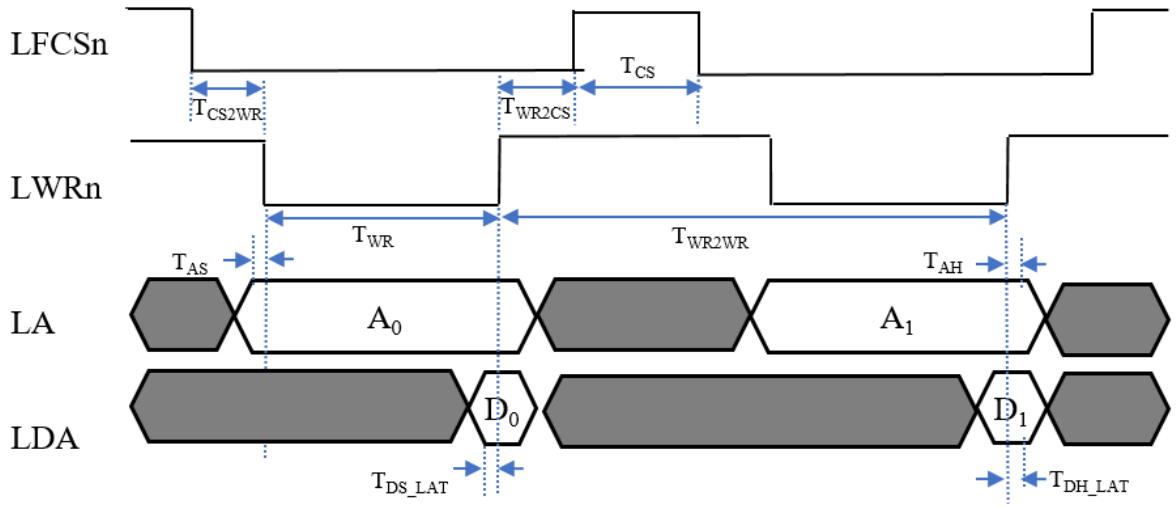

Figure 4-33: Function Local Bus Write Access (Late Sample = 1)

Table 4-19: Function Local Bus Access Timing

Symbol	Description	Min	Typ	Max	Units
T_{CS}	LFCSn back to back	30	-	-	ns
T_{CS2RD}	LFCSn to LRDn	0	-	-	ns
T_{CS2WR}	LFCSn to LWR,	0	-	-	ns
T_{RD2CS}	LRDn to LFCSn	0	-	-	ns
T_{WR2CS}	LWRn to LFCSn	0	-	-	ns
T_{AS}	LA setup time	0	-	-	ns
T_{AH}	LA hold time	0	-	-	ns
T_{A2D}	LA change to LDA valid	-	-	40	ns
T_{RD}	LRDn pulse	T_{RD2D}	-	-	ns
T_{RD2D}	LRDn to LRDY	-	-	80	ns
T_{WR}	LWRn pulse	30	-	-	ns
T_{WR2RDY}	LWRn assert to LRDY assert	-	-	60	ns
T_{WR2WR}	LWRn back to back (late sample)	100	-	-	ns
T_{DS_NOR}	LDA setup time	0	-	-	ns
T_{DH_NOR}	LDA hold time	40	-	-	ns
T_{DS_LAT}	LDA setup time with Late Sample	10	-	-	ns
T_{DH_LAT}	LDA hold time with Late Sample	10	-	-	ns

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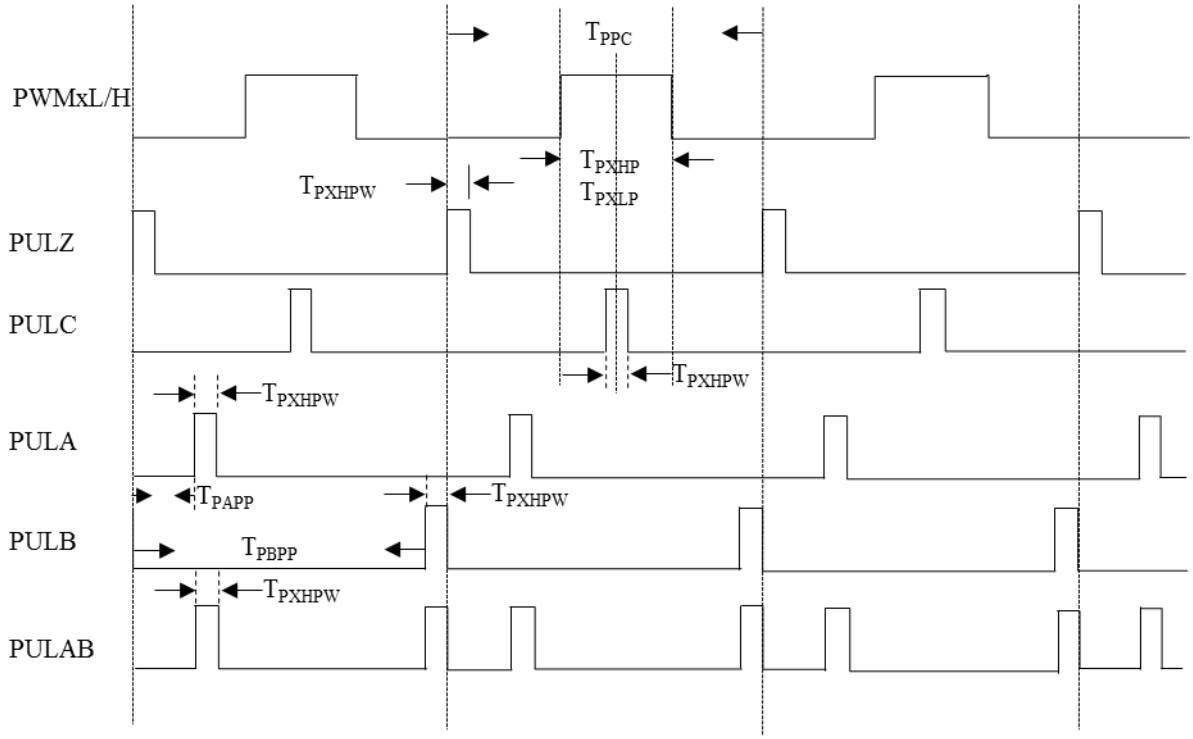
4.5.9 PWM Motor Controller Timing



Note: PWMx mean PWM 1 to PWM 3

Figure 4-34: PWMx Timing

Table 4-20: PWMx Timing Table

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{PPC}	PWM Period Cycle	x1	-	PPC * 10	-	ns
		x8	-	PPC * 80	-	ns
T_{PxHP}	PWM x High pulse Width set by PxHPWR	x1	-	PxHPV * 10*1	-	ns
		x8	-	PxHPV * 80*1	-	ns
T_{PxLP}	PWM x Low pulse Width set by PxHPWR	x1	-	PxHPV * 10*1	-	ns
		x8	-	PxHPV * 80*1	-	ns
T_{PXHPW}	Pulse width for PULZ, PULC, PULA, PULB, and PULAB	x1	-	PXHPW * 10	-	ns
		x8	-	PXHPW * 80	-	ns
T_{PAPP}	PWM Trigger Pulse A Position in PWM Period Cycle	x1	-	PTAPP * 10	-	ns
		x8	-	PTAPP * 80	-	ns
T_{PBPP}	PWM Trigger Pulse B Position in PWM Period Cycle	x1	-	PTBPP * 10	-	ns
		x8	-	PTBPP * 80	-	ns

Note *1: “x” = 1 ~ 3

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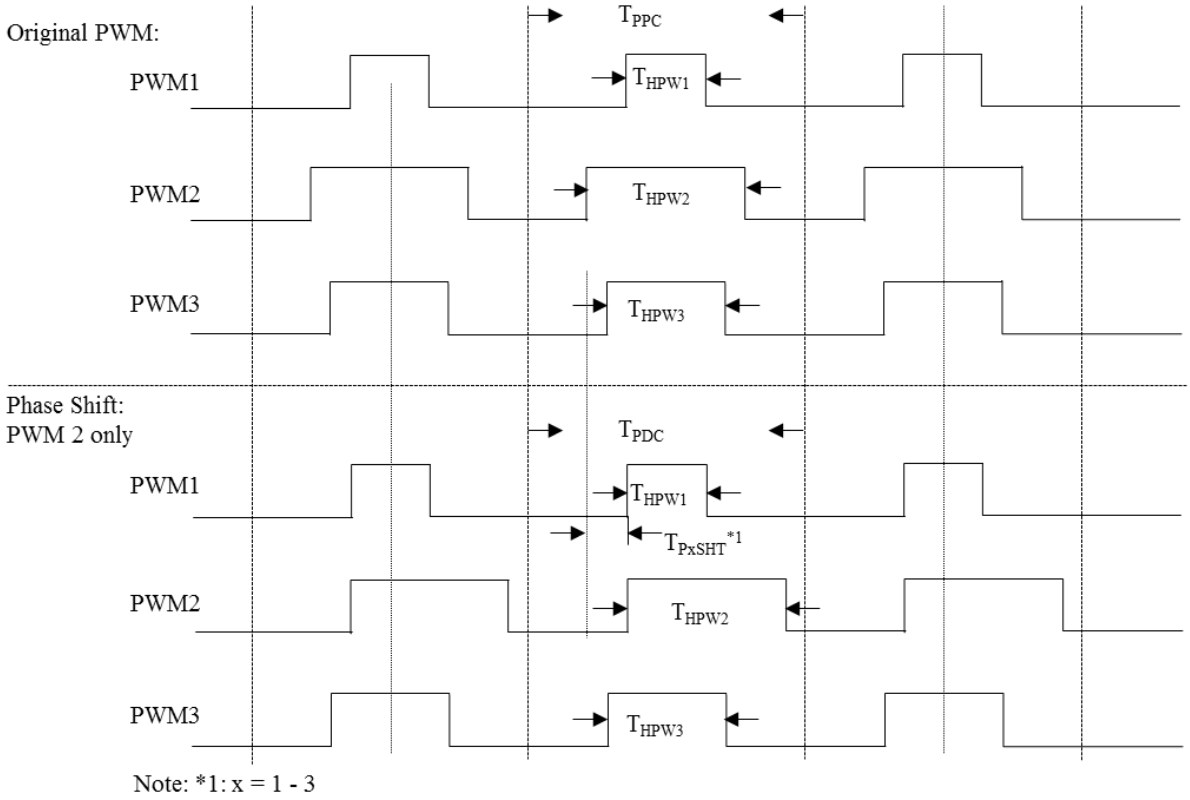

Figure 4-35: Only PWM Channel 2 Shift Diagram

Table 4-21: PWMx Shift Timing Table

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{P1SHT}	PWM pulse was postponed raising time (addition with P1SHR) and the pulse width stays the same	x1	-	P1SHIFT * 10	-	ns
		x8	-	P1SHIFT * 80	-	ns
T_{P2SHT}	Please reference T_{P1SHT} content	x1	-	P2SHIFT * 10	-	ns
		x8	-	P2SHIFT * 80	-	ns
T_{P3SHT}	Please reference T_{P1SHT} content	x1	-	P3SHIFT * 10	-	ns
		x8	-	P3SHIFT * 80	-	ns

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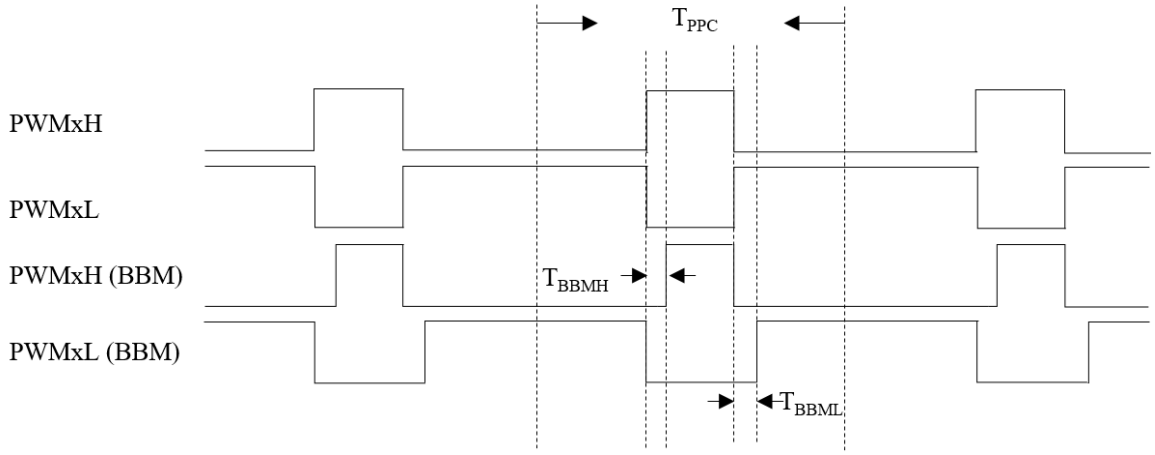

Figure 4-36: BBM (Break Before Make) Timing Diagram

Table 4-22: PWMx BBM Timing Table

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{BBMH}	High pulse was postponed raising and reduce pulse width	x1	-	PBBMH * 10	-	ns
		x8	-	PBBMH * 80	-	ns
T_{BBML}	Low pulse was postponed falling and addition pulse width	x1	-	PBBML * 10	-	ns
		x8	-	PBBML * 80	-	ns

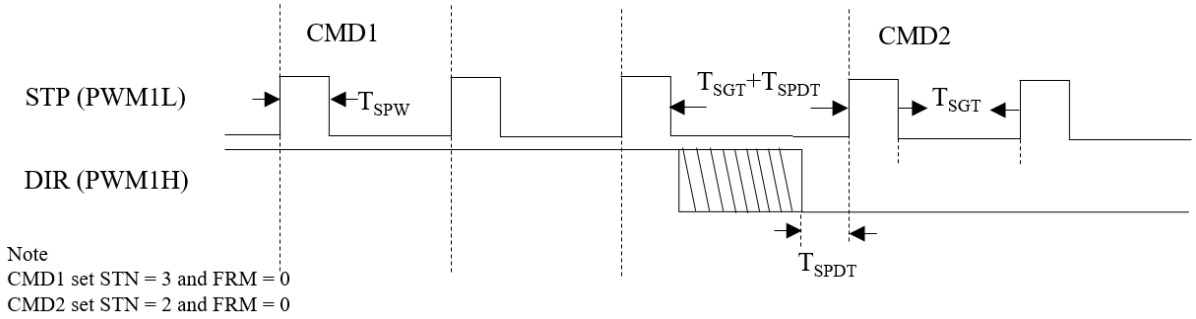

Figure 4-37: One Shot with multi–Step Timing Diagram

Table 4-23: Step function timing table

Symbol	Description	Min	Typ	Max	Units
T_{SGT}	Step Pulse to Pulse Gap time set by SGTLR and SGTHR	-	SGT * 10	-	ns
T_{SPW}	Step Pulse Width set by SHPWR Note: Step frequency = 1/ (T_{SPW} +T_{SGT})	-	SPW * 10	-	ns
T_{SPDY}	Direction Transform Delay Time set by TDLYR	-	SPDT * 10	-	ns

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4.5.10 Incremental and Hall Encoder Interface Timing

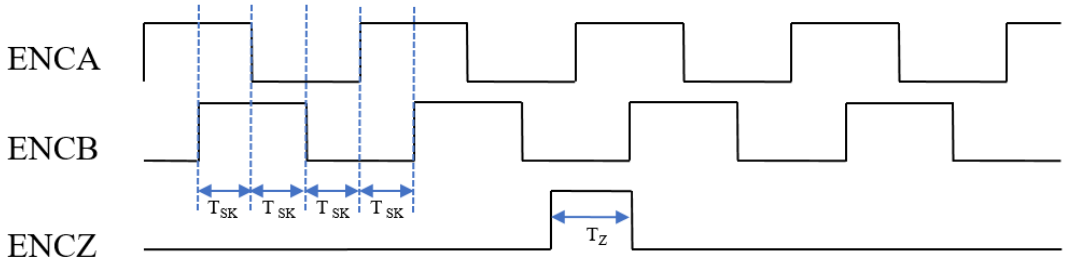

Figure 4-38: ABZ Timing Diagram

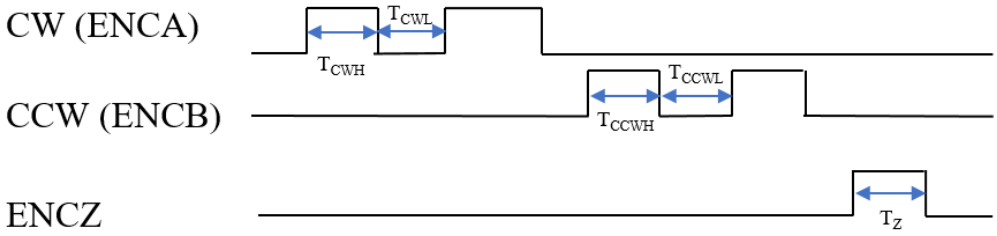

Figure 4-39: CW/CCW Timing Diagram

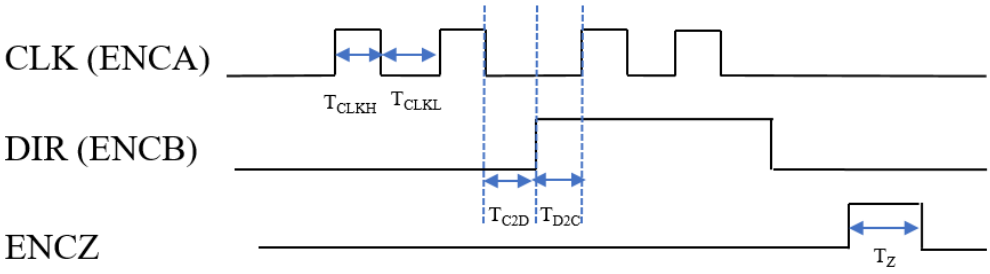

Figure 4-40: CLK/DIR Timing Diagram

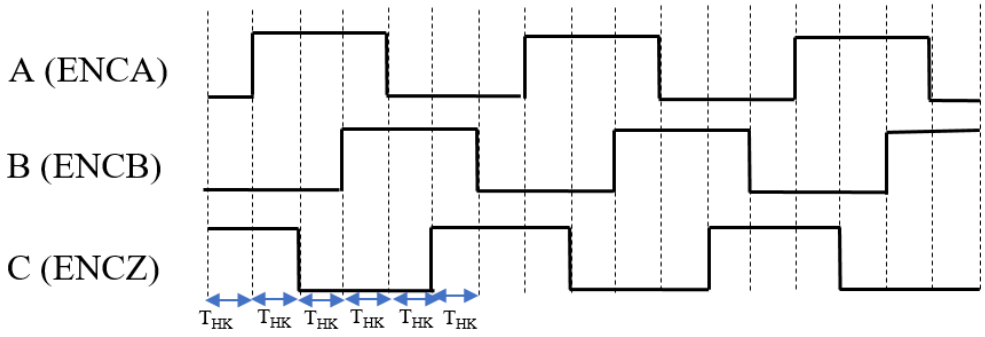

Figure 4-41: Hall Timing Diagram

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Table 4-24: Incremental and Hall Encoder Timing Table

Symbol	Description	Min	Typ	Max	Units
T_{SK}	AB state keep time	30	-	-	ns
T_Z	Z Pulse Width	30	-	-	ns
T_{CWH}	CW high time	30	-	-	ns
T_{CWL}	CW low time	30	-	-	ns
T_{CCWH}	CCW high time	30	-	-	ns
T_{CCWL}	CCW low time	30	-	-	ns
T_{CLKH}	CLK high time	30	-	-	ns
T_{CLKL}	CLK low time	30	-	-	ns
T_{C2D}	CLK to DIR time	30	-	-	ns
T_{D2C}	DIR to CLK time	30	-	-	ns
T_{HK}	Hall state keeps time	60	-	-	ns

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4.5.11 SPI Master Timing

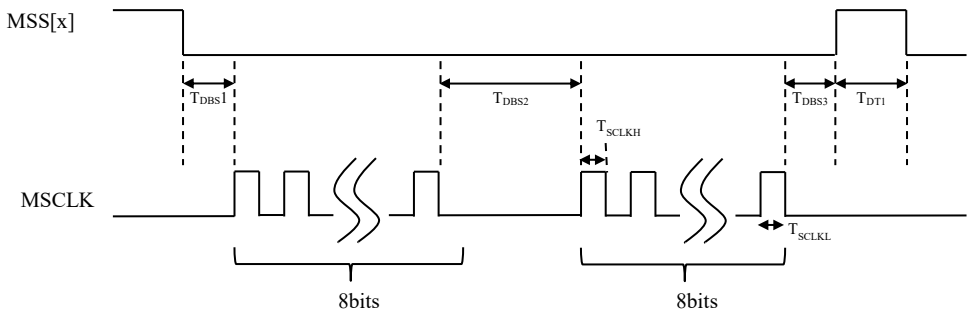

Figure 4-42: SPI Master Timing

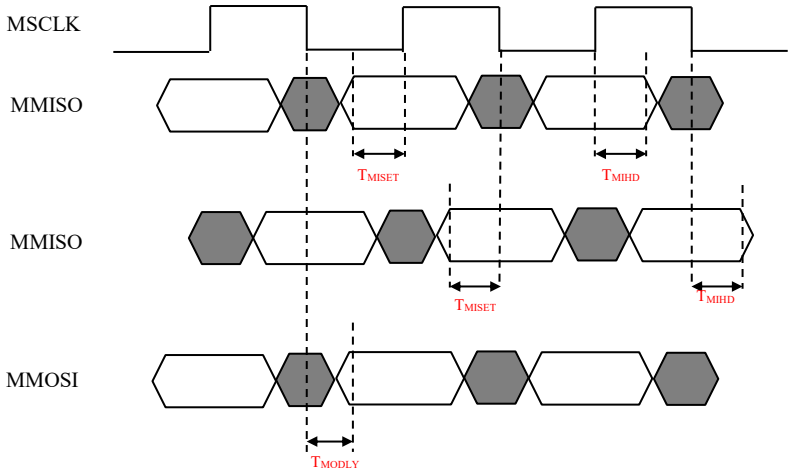

Figure 4-43: MMISO /MMOSIO Timing

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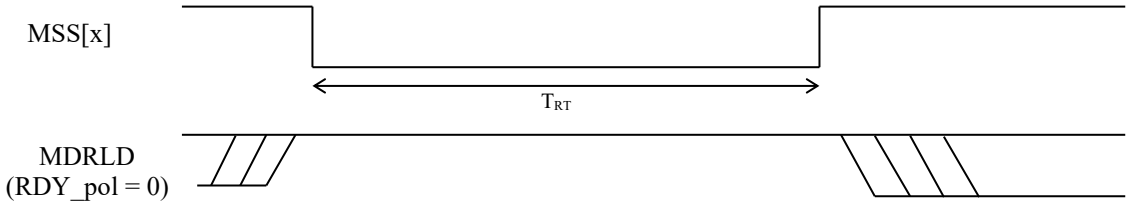

Figure 4-44: SPI MDRLD Ready Timeout Timing

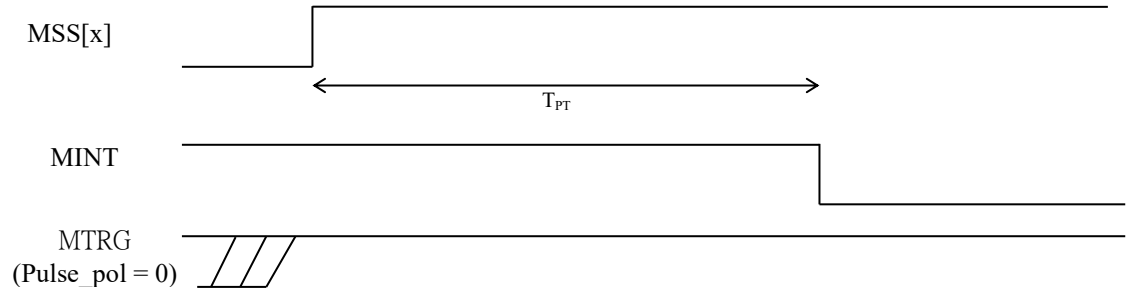

Figure 4-45: SPI MTRG Trigger Pulse Timeout

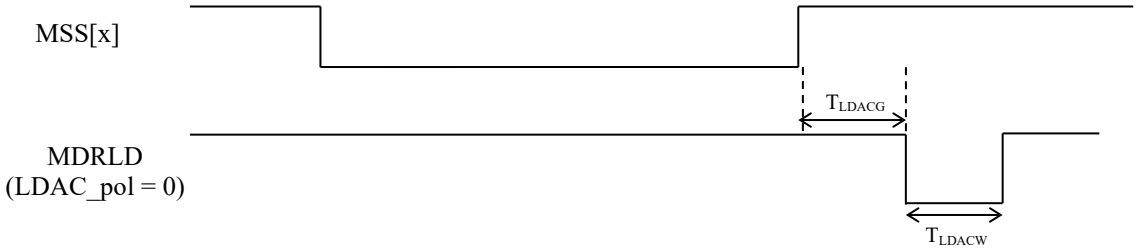

Figure 4-46: SPI MDRLD Trigger LDAC Gap and Width Timing

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Table 4-25: SPI Master Timing Table

Symbol	Description	Min	Typ	Max	Units
Clock					
T_{SCLK}	MSCLK Period	-	T_{SCLKH} + T_{SCLKL}	-	ns
T_{SCLKH}	MSCLK high	-	5 * Divide	-	ns
T_{SCLKL}	MSCLK low	-	5 * Divide	-	ns
Bus Timing					
T_{DBS1}	MSS[x] to MSCLK (Mode0/1 without DBS1K)	-	(DBS + 1) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode2/3 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 1) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
T_{DBS2}	Byte to byte (Mode0/1 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	Byte to byte (Mode2/3 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	Byte to byte (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
	Byte to byte (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
T_{DBS3}	MSCLK to MSS[x] (Mode0/1 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode2/3 without DBS1K)	-	(DBS + 1.0) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 1.0) * Tsclk	-	ns
T_{DT1}	MSS[x] gap (without DT1K)	-	(DT + 2) * Tsclk	-	ns
	MSS[x] gap (with DT1K)	-	(1024 * (DT + 1) + 2) * Tsclk	-	ns
T_{MISET}	MMISO setup time	10.5	-	-	ns
T_{MIHD}	MMISO hold time	0	-	-	ns
T_{MODLY}	MMOSI output delay	-	-	0.5	ns
T_{RT}	MDRLD ready timeout (RDY mode)	-	(1 + SPIRPT) * 1024 * Tsclk	-	ns
T_{PT}	MTRG timeout	-	(1 + SPIRPT) * 1024 * Tsclk	-	ns
T_{LDACG}	MDRLD Gap (LDAC mode)	-	((LDACG1K * 1023) + 1) * (LDGAP + 1) * Tsclk	-	ns
T_{LDACW}	MDRLD Width (LDAC mode)	-	(LDACG1K * 1023 + 1) * (LDWID + 1) * Tsclk	-	ns

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4.5.12 RSTO, CLKOUT, EEPROM and EEP_DONE Timing

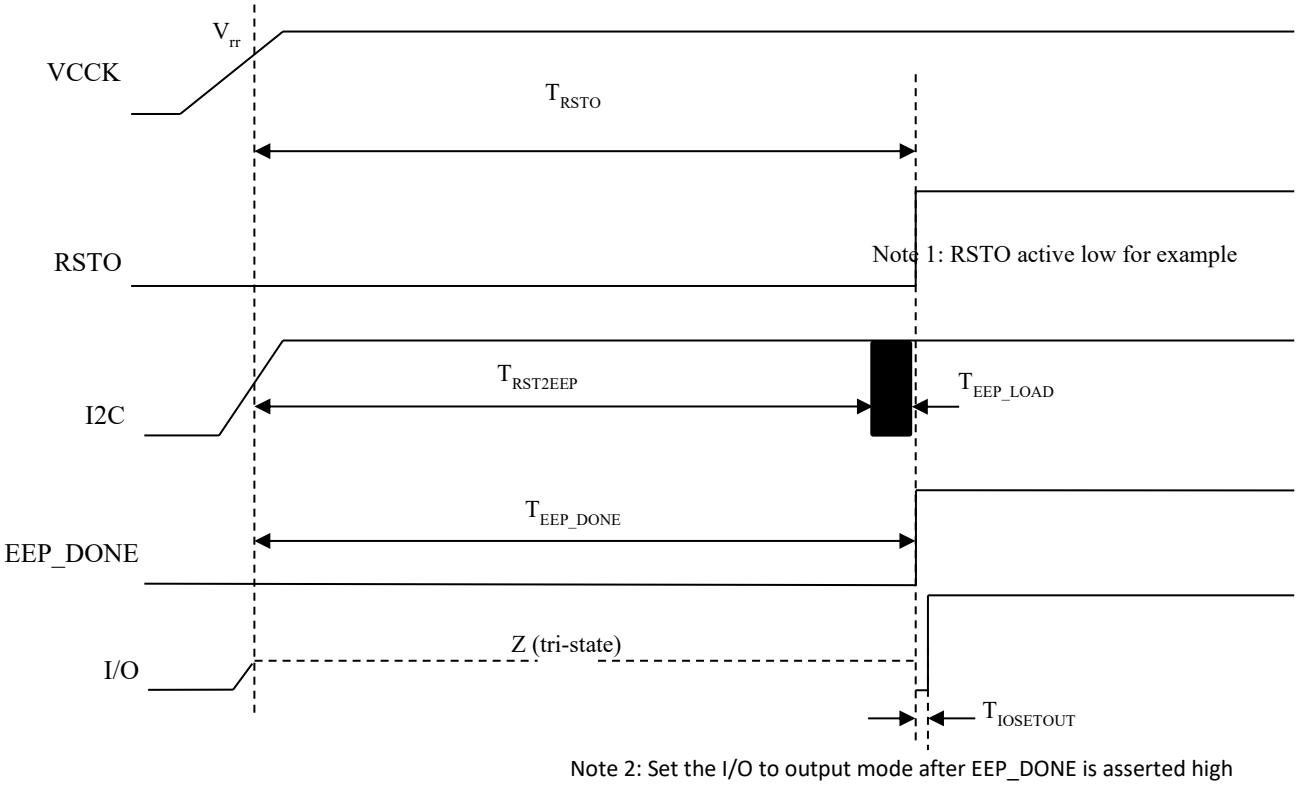

Figure 4-47: Power up to RSTO, EEPROM and EEP_DONE Timing

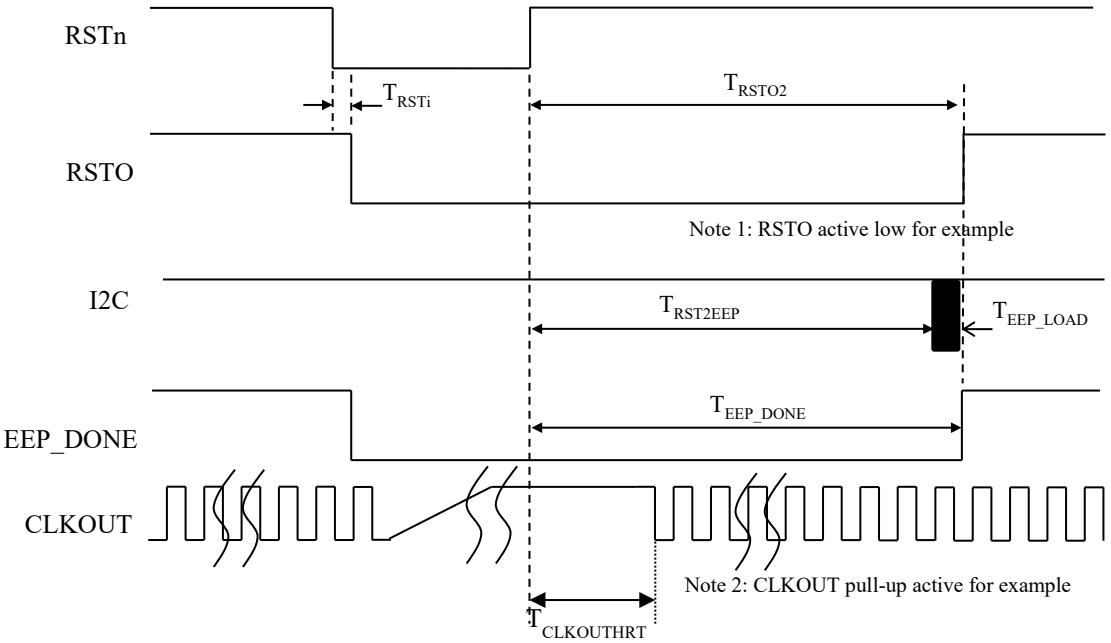

Figure 4-48: RSTn to RSTO, EEPROM and EEP_DONE Timing

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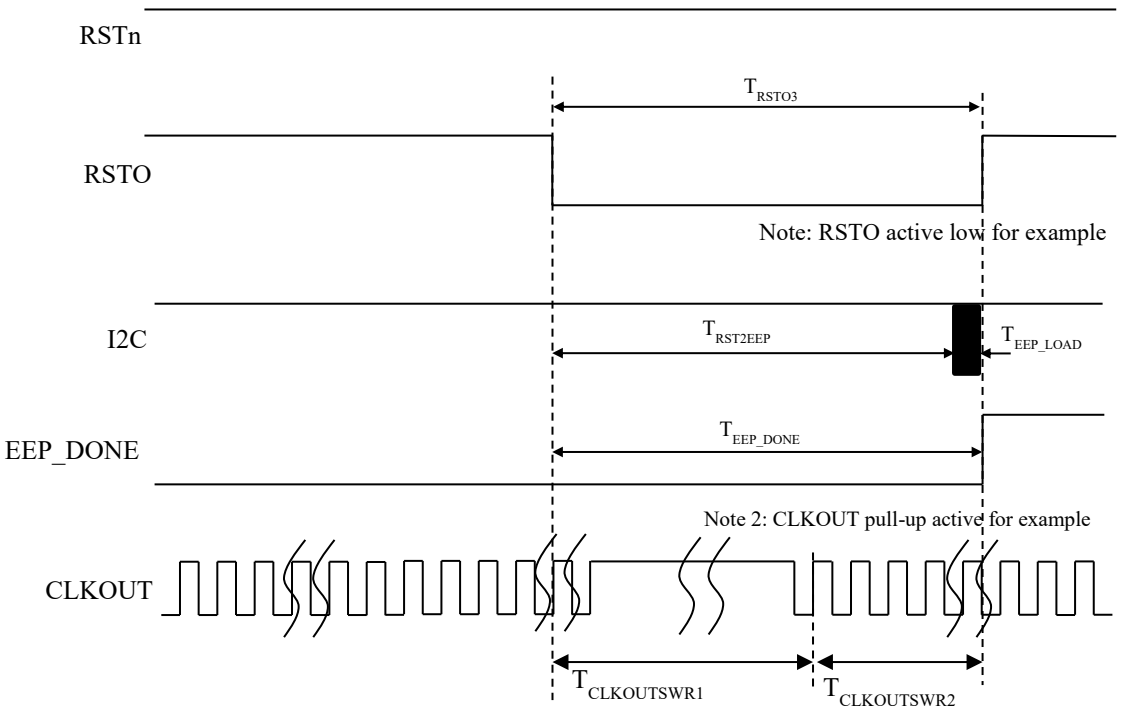

Figure 4-49: Register Reset to RSTO, EEPROM and EEP_DONE Timing

Table 4-26: RSTO, EEPROM and EEP_DONE timing table

Symbol	Description	Min	Typ	Max	Units
T_{RSTO1}	Once VCCK reaches V_{rr}, RSTO de-asserted	-	10.6	-	ms
T_{RSTO2}	RSTn de-asserted to RSTO	-	7.4	-	ms
T_{RSTO3}	The period of chip internal reset counter	-	8.7	-	ms
T_{RSTi}	RSTn asserted to RSTO active	-	110	-	ns
$T_{RST2EEP}$	RSTn de-asserted to start EEPROM Loading	-	5.9	-	ms
T_{EEP_LOAD}	EEPROM loading period (Checksum Matched)	-	1.5	-	ms
T_{EEP_DONE}	RSTn de-asserted to EEP_DONE active	-	9.4	-	ms
$T_{IOSETOUT}$	The output enable is asserted after EEP_DONE goes high	-	40	-	ns
$T_{CLKOUTHRT}$	RSTn de-asserted to CLKOUT	-	5.4	-	ms
$T_{CLKOUTSRT1}$	The CLKOUT output stops after executing the ESC reset command	-	7	-	ms
$T_{CLKOUTSRT2}$	Initiates CLKOUT output after executing the ESC reset command	-	6	-	ms

Note**:** The ESC reset command is executed by writing to the “ESC Reset ECAT” or “ESC Reset PDI” register.

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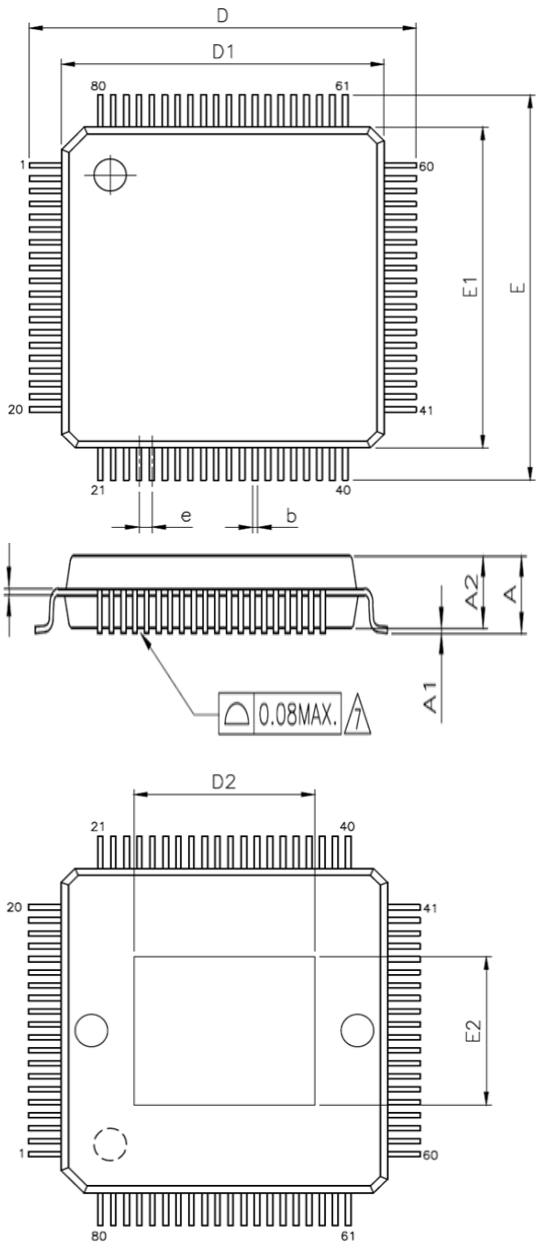
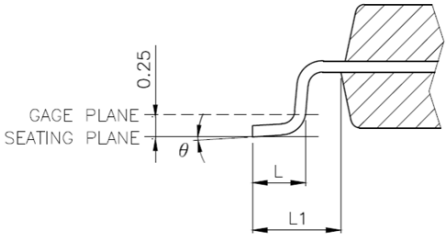
5 Package Information

5.1 LQFP80



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	D2		E2	
	MIN.	MAX.	MIN.	MAX.
21*X18*	4.71	5.69	3.88	4.72

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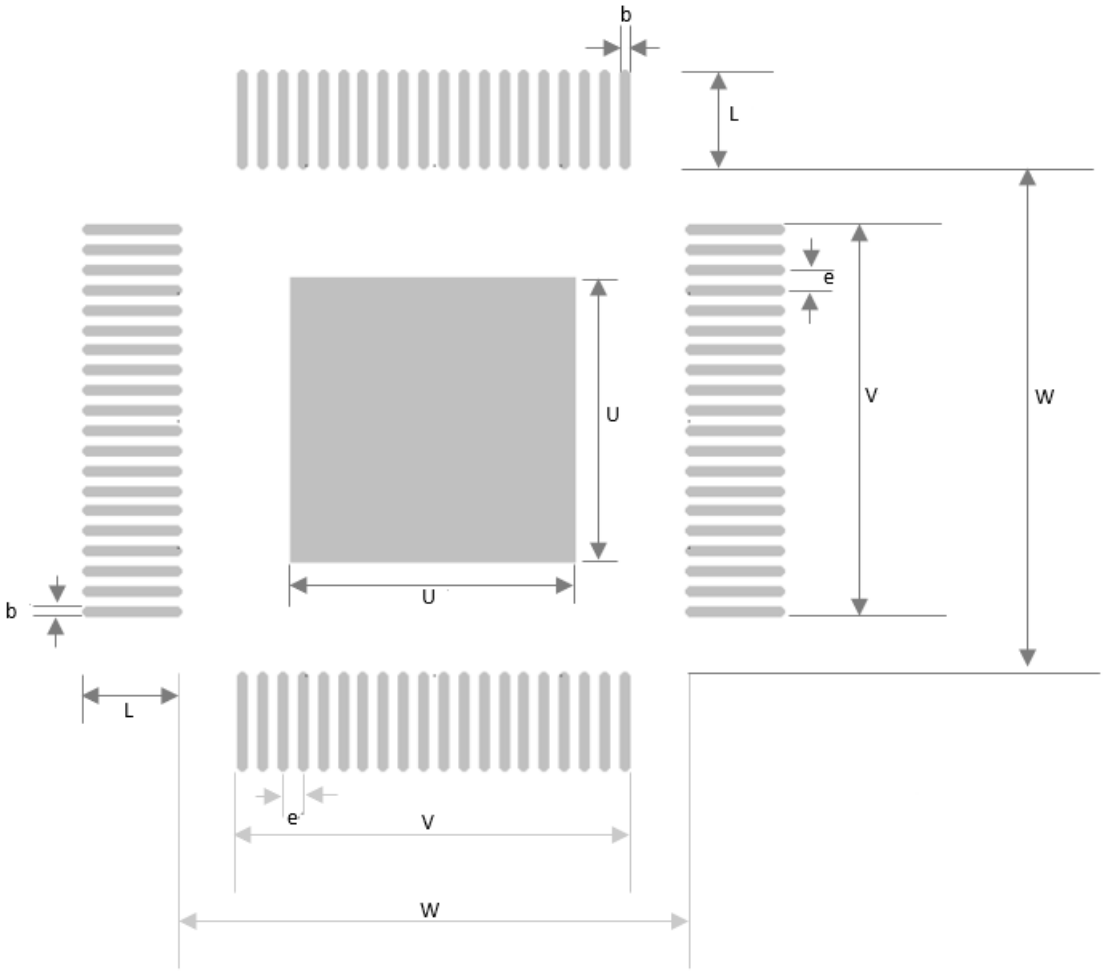
Recommended PCB Footprint for 80-pin LQFP Lead Free Package



Symbol	Description	Typical Dimension
e	Lead pitch	0.40 mm
b	Pad width	0.20 mm
L	Pad length	2.00 mm
U	-	5.70 mm
V	-	7.80 mm
W	-	10.00 mm

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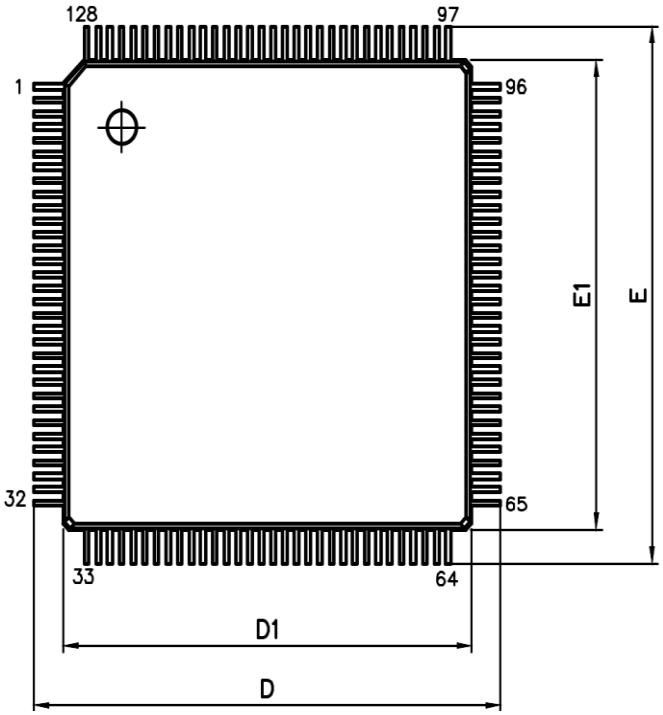
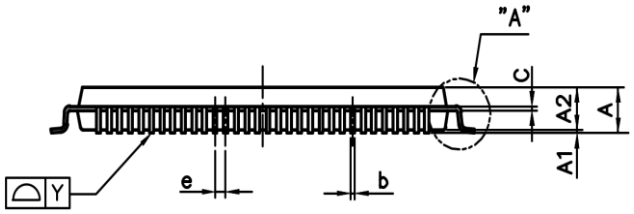
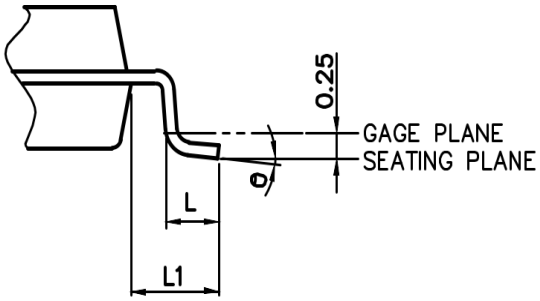
5.2 LQFP128

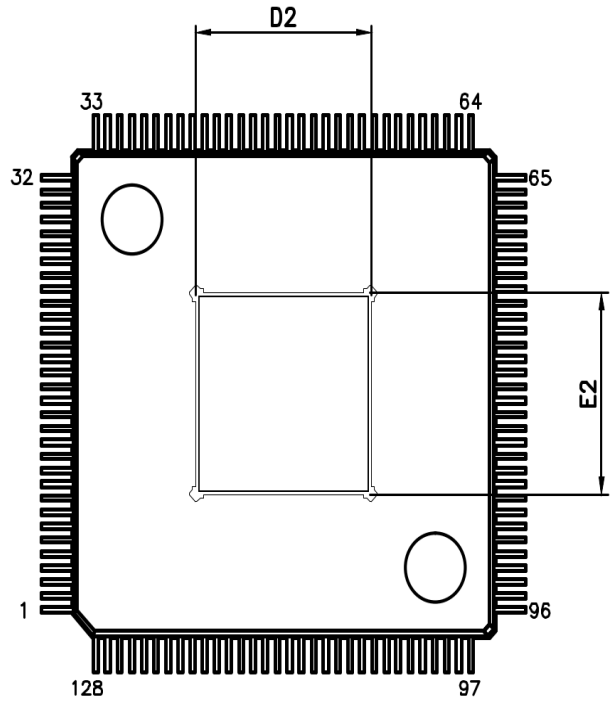


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	--	0.23
c	0.09	--	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
Y	0.08		







THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	D2		E2	
	MIN.	MAX.	MIN.	MAX.
23*X23* MIL	5.79	5.99	5.79	5.99

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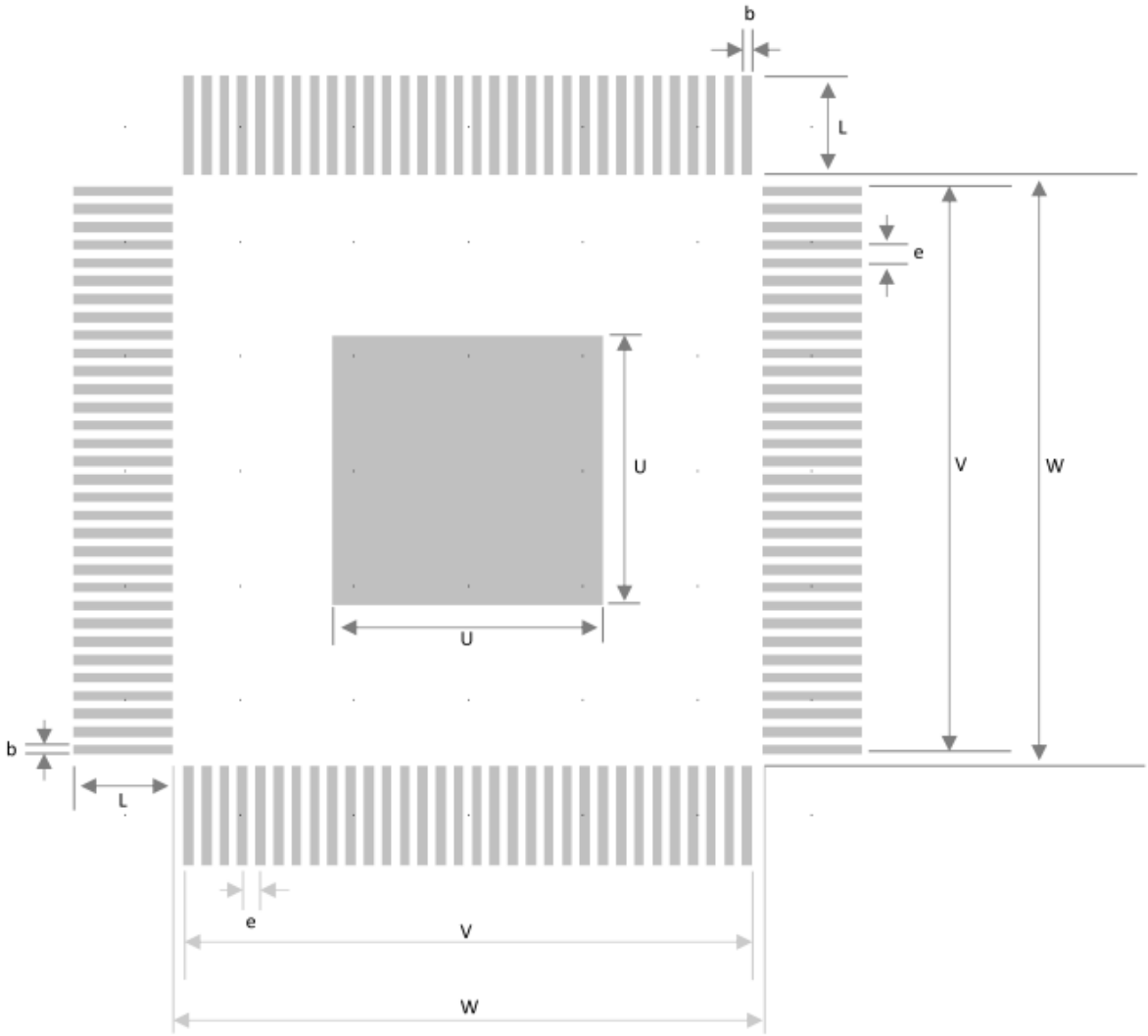
Recommended PCB Footprint for 128-pin LQFP Lead Free Package



Symbol	Description	Typical Dimension
e	Lead pitch	0.40 mm
b	Pad width	0.20 mm
L	Pad length	2.20 mm
U	-	6.00 mm
V	-	12.60 mm
W	-	13.10 mm

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6 Ordering Information

Part Number	Description
AX58101 LT	80-pin LQFP lead Free package, Industrial temperature range: -40 to 105°C.
AX58102 LT	128-pin LQFP lead Free package, Industrial temperature range: -40 to 105°C.

7 Revision History

Revision	Date	Comments
1.00	2025/07/30	Initial release.
1.01	2026/01/28	1. Updated PDI LB AD merge mode description, 2. Updated ESC PDI Local Bus Timing in Section 4.5.7 3. Updated power consumption in Section 4.2

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