

**AX58100 Migration from Beckhoff ET1100  
Application Note**

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# AX58100 Migration from Beckhoff ET1100 Application Note

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## Revision History

Revision	Date	Description
1.00	2018/12/05	Initial release

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## 1. Introduction

This document indicates the hardware/software design notes to migrate from Beckhoff ET1100 ESC solution to AX58100 ESC solution.

## 2. Functions Overview

The AX58100 is a 2/3-port EtherCAT Slave Controller (ESC), licensed from Beckhoff Automation, with two integrated Fast Ethernet PHYs which support 100Mbps full-duplex operation and HP Auto-MDIX. AX58100 supports 9 Kbytes Process Data RAM, 8 Fieldbus Memory Management Units (FMMUs), 8 Sync-Managers and a 64-bit Distributed Clock.

Compared to other EtherCAT slave controller solutions, the AX58100 integrates two embedded Fast Ethernet PHYs which can support both copper and fiber industrial Ethernet applications and supports some additional interfaces such as Pulse Width Modulation (PWM), Incremental (ABZ)/Hall Encoder, SPI master, 32 Digital I/O, Emergency Stop Input, etc. for designers to easily implement AX58100 on different EtherCAT industrial fieldbus applications without extra microprocessor. The AX58100 provides SPI slave and Local bus Process Data Interfaces (PDI) to provide an easy way for system designers to implement the standard EtherCAT communication functionalities on those traditional non-EtherCAT MCU and DSP industrial platforms.

The AX58100 provides a cost-effective EtherCAT slave controller solution for industrial automation, motion/motor/Digital IO control, Digital to Analog (DAC)/Analog to Digital (ADC) converters control, sensors data acquisition, robotics, etc. industrial Ethernet fieldbus applications.

The following is the major features comparison between AX58100 and Beckhoff ET1100 ESC solutions.

Part No.	Ethernet Ports	FMMU	Sync Managers	RAM (Kbytes)	Distributed Clock	Digital I/O	SPI Slave
AX58100	2 x PHY 1 x MII	8	8	9	64 bits	32 bits	Yes
ET1100	2-4 (Each EBUS/II)	8	8	8	64 bits	32 bits	Yes

Part No.	Local Bus	SPI Master	PWM/ Step-DIR	ABZ/Hall Encoder	Emergency Stop Input	Temperature Range (°C)	Package
AX58100	8/16 bit Async	Yes	Yes	Yes	Yes	-40 ~ +105	LQFP-80
ET1100	8/16 bit Sync/Async	No	No	No	No	-40 ~ +85	BGA-128

Table 2-1. Major Features Comparison between AX58100 and ET1100

### 2-1. Block Diagram

The following are the block diagrams of AX58100 and ET1100.

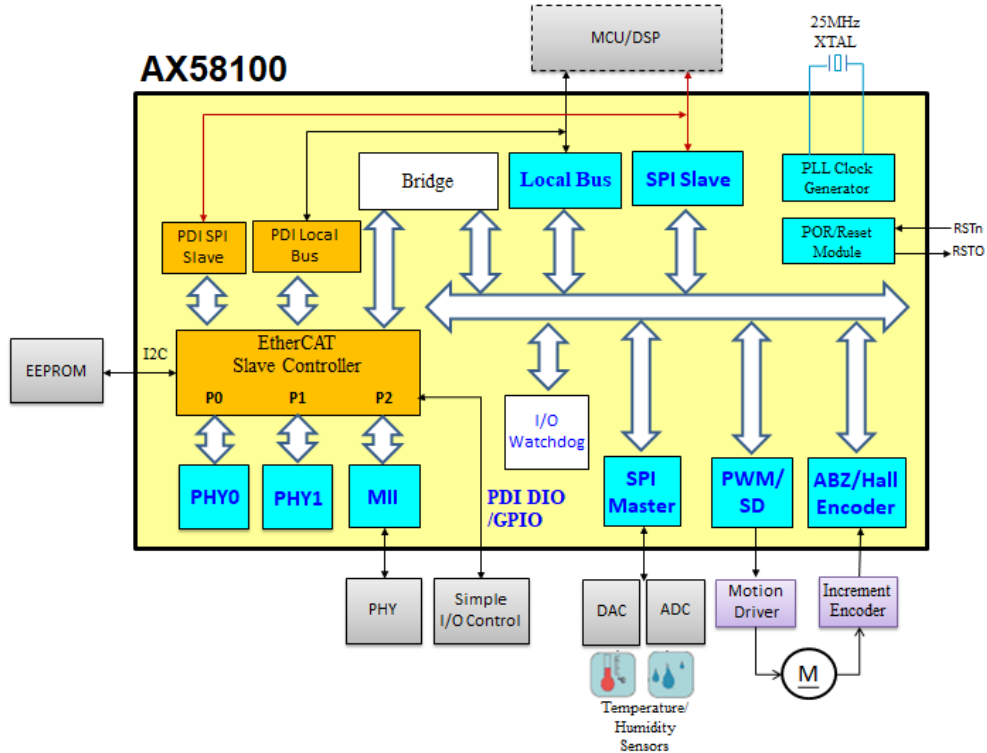


Figure 2-1. AX58100 Block Diagram

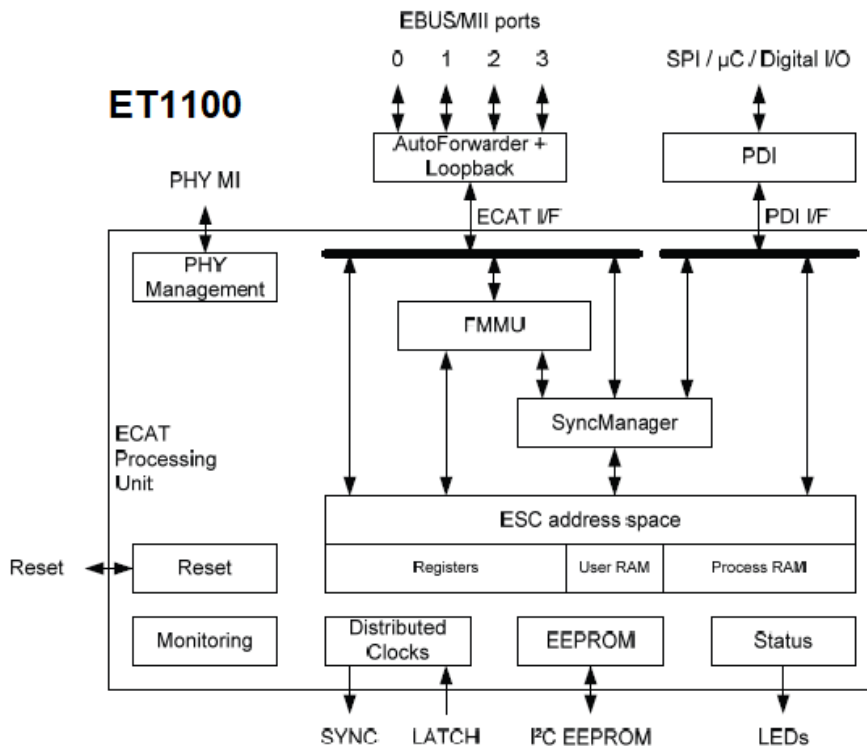


Figure 2-2. ET1100 Block Diagram

## 2-2. Application Diagram

The following are the typical applications diagrams of AX58100 and ET1100. The AX58100 integrates additional interfaces such as Pulse Width Modulation (PWM), ABZ/Hall Encoder, SPI master, 32 Digital I/O, Emergency Stop Input, etc. for designers to easily implement AX58100 on different EtherCAT industrial fieldbus applications without extra microprocessor.

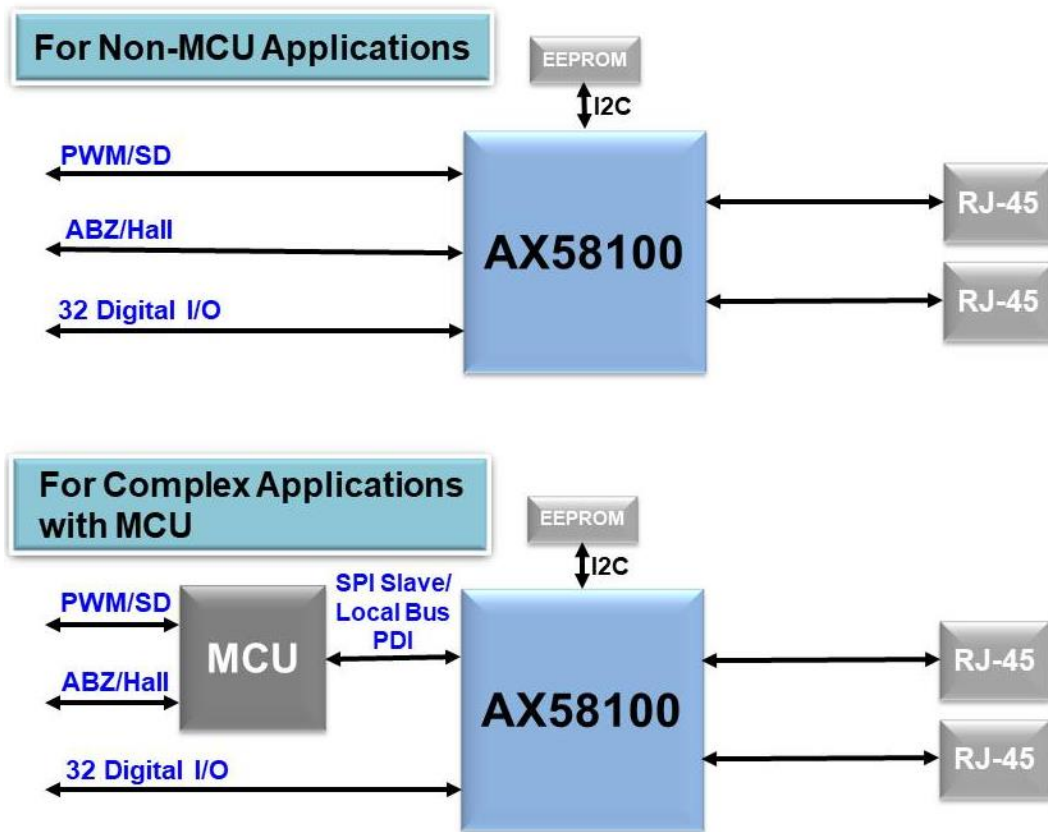


Figure 2-3. AX58100 Application Diagram

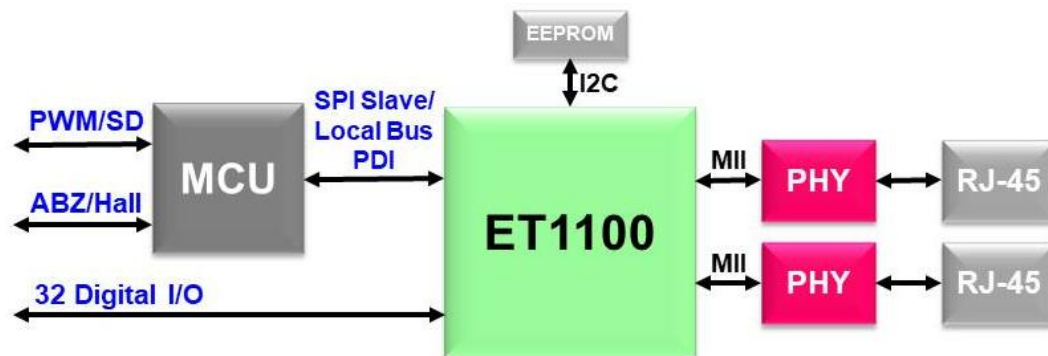


Figure 2-4. ET1100 Application Diagram

## 3. Hardware Transition

This section indicates the hardware design considerations while migrating from Beckhoff ET1100 ESC solution to AX58100 ESC solution.

### 3-1. Bootstrap Hardware Configuration Pins

The AX58100 supports five multi-function bootstrap pins (pin 19, 20, 58, 40, and 41) for five hardware configurations, i.e. external I2C EEPROM size, ESC supported port number, RSTO polarity and integrated port 0/1 PHY media mode; and supports other three multi-function bootstrap pins (pin 42, 52, 66) for the configuration of port 2 MII signals. User needs to utilize an external resistor to pull up/down these bootstrap pins for correct AX58100 hardware configuration.

Beckhoff supports different hardware configuration pins based on the ET1100 product design specification. Please refer to *Beckhoff ET1100 datasheet* for details.

Pins	Signal Name	Description
19	EEP_SIZE	I <sup>2</sup> C EEPROM Size 0: 1 Kbit to 16Kbit 1: 32Kbit to 4Mbit
20	3PORT_MODE	ESC port number 0: 2 ports mode (Port 0, 1) 1: 3 ports mode (Port 0, 1 & 2)
58	RSTO_POL	RSTO Reset Output Polarity 0:Active Low 1:Active High
40	P0_FIBER	Port 0 PHY media mode 0: Copper mode 1: Fiber mode
41	P1_FIBER	Port 1 PHY Media mode 0: Copper mode 1: Fiber mode
66	TX_SH[1]	Port 2 MII TXD Align position 2'b00: Align with MCLK, 2'b01: Delay 1/4 phase with MCLK 2'b10: Delay 1/2 phase with MCLK 2'b11: Delay 3/4 phase with MCLK
42	TX_SH[0]	
52	LINK_POL	Port 2 MII LINK Polarity 0:Active Low 1:Active High

Table 3-1. AX58100 Bootstrap Configuration Pins

### 3-2. Ethernet Ports

The AX58100 ESC, which is licensed from Beckhoff Automation, supports two embedded PHYs and an optional MII interface for flexible network topology. The embedded Fast Ethernet PHYs support 100Mbps full-duplex operation and HP Auto-MDIX, and are fully compliant with the 100BASE-TX and 100BASE-FX Ethernet standards such as IEEE 802.3u, and ANSI X3.263-1995 (FDDI-TP-PMD) for both copper and fiber industrial Ethernet applications.

The optional MII interface of AX58100 ESC is optimized for low processing/forwarding delays by omitting a transmit FIFO. To allow this, the ESC has additional requirements to Ethernet PHY, which is easily accomplished by several PHY vendors. Please refer to *Beckhoff's PHY Selection Guide* to select a proper Ethernet PHY.

AX58100 Port 0 and Port 1 integrate embedded Ethernet PHYs, and Port 2 is an optional MII interface which are multi-function pins shared with others interfaces (i.e. PWM, Hall, Local Bus, Digital I/O). Packets are forwarded in the following order:

**Port 0 -> EtherCAT Processing Unit -> Port 1 -> Port 2**

AX58100 supports six Bootstrap pins (pin 20, 40-42, 52 and 66) for Ethernet ports hardware configurations. Please refer to [Table 3-1](#) for details.

The following is the principle connection between AX58100 Port 2 MII interface and Ethernet PHY. The clock source of the Ethernet PHYs and ESC must be the same quartz. The TX\_CLK is not connected because the ESCs do not incorporate a TX FIFO. The TX signals can be delayed inside the ESC by setting AX58100 TX\_SH[1:0] bootstrap pins for TX\_CLK phase shift compensation. The LINK is connected to the PHY LED output indicating a 100 Mbps (Full Duplex) link.

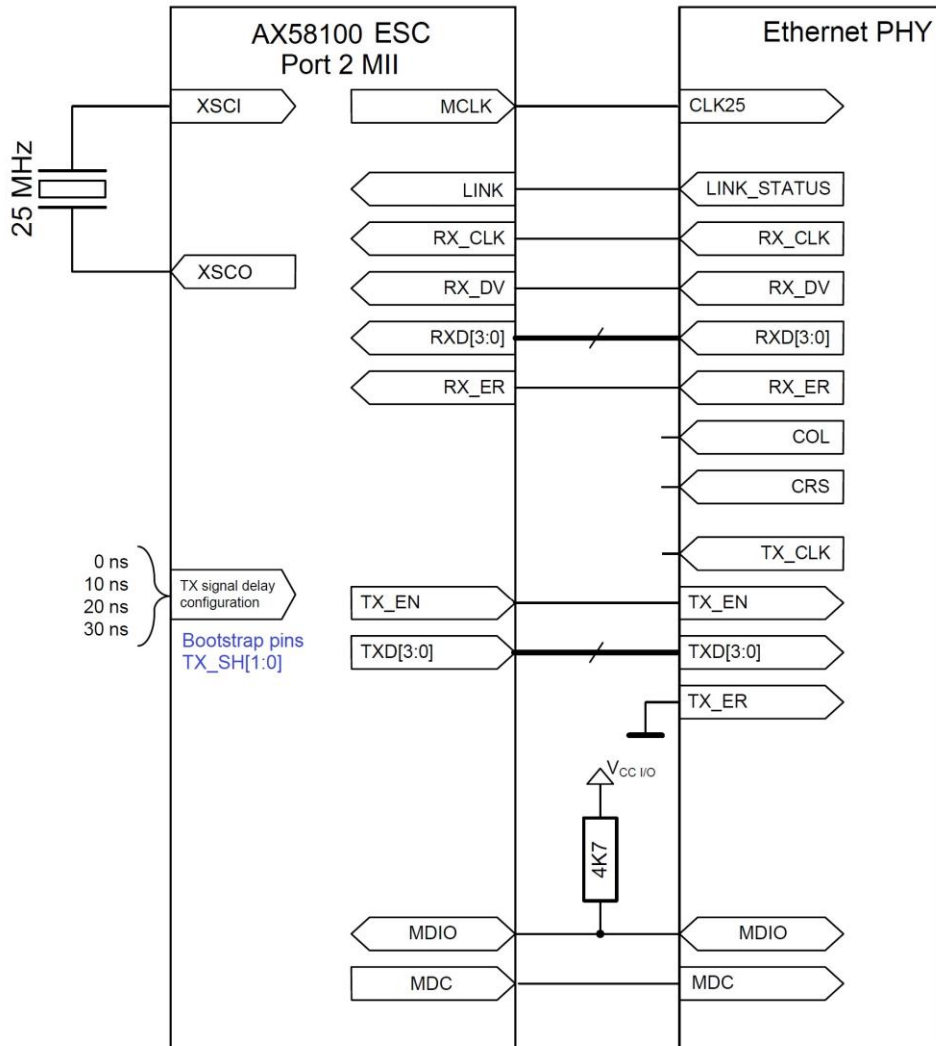


Figure 3-1. The principle connection between AX58100 Port 2 MII interface and Ethernet PHY

### 3-3. Digital I/O PDI

The following are the hardware transition notes for Digital I/O applications to migrate from Beckhoff ET1100 to AX58100.

1. AX58100 doesn't support the OE\_CONF pin function of ET1100. The AX58100 Digital I/O Output Enable function is configured by setting the OE\_EXT pin directly.
2. AX58100 supports the EOF pin for End of Frame signal.
3. The EEP\_DONE signal is optional to indicate the ESC PDI bus is active.

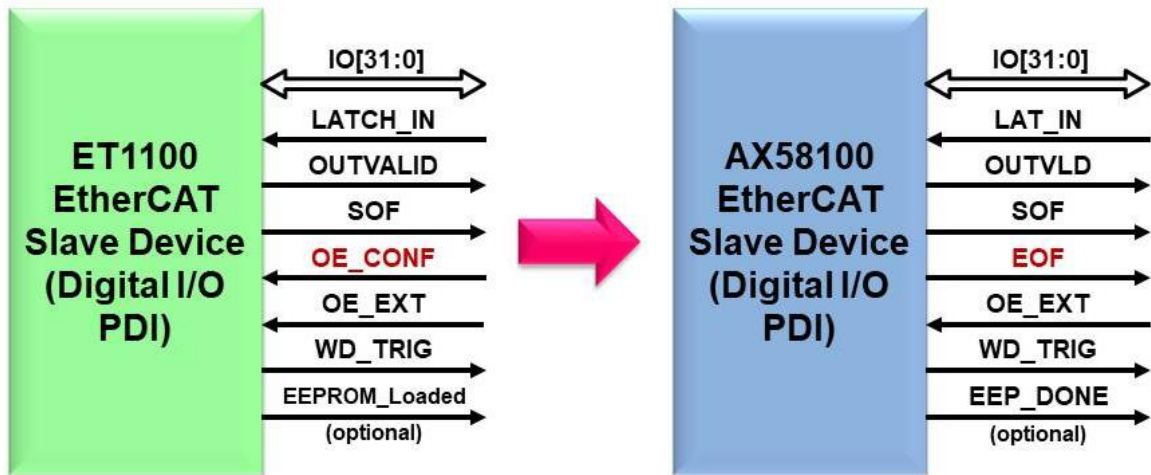


Figure 3-2. Digital I/O PDI Interface Hardware Transition

### 3-4. SPI Slave PDI

The following are the hardware transition notes for SPI Slave PDI applications to migrate from Beckhoff ET1100 to AX58100.

1. Pull high the SCS\_FUNC signal via a 4.7K Ohm resistor.
2. The EEP\_DONE signal is optional to indicate the ESC PDI bus is active.

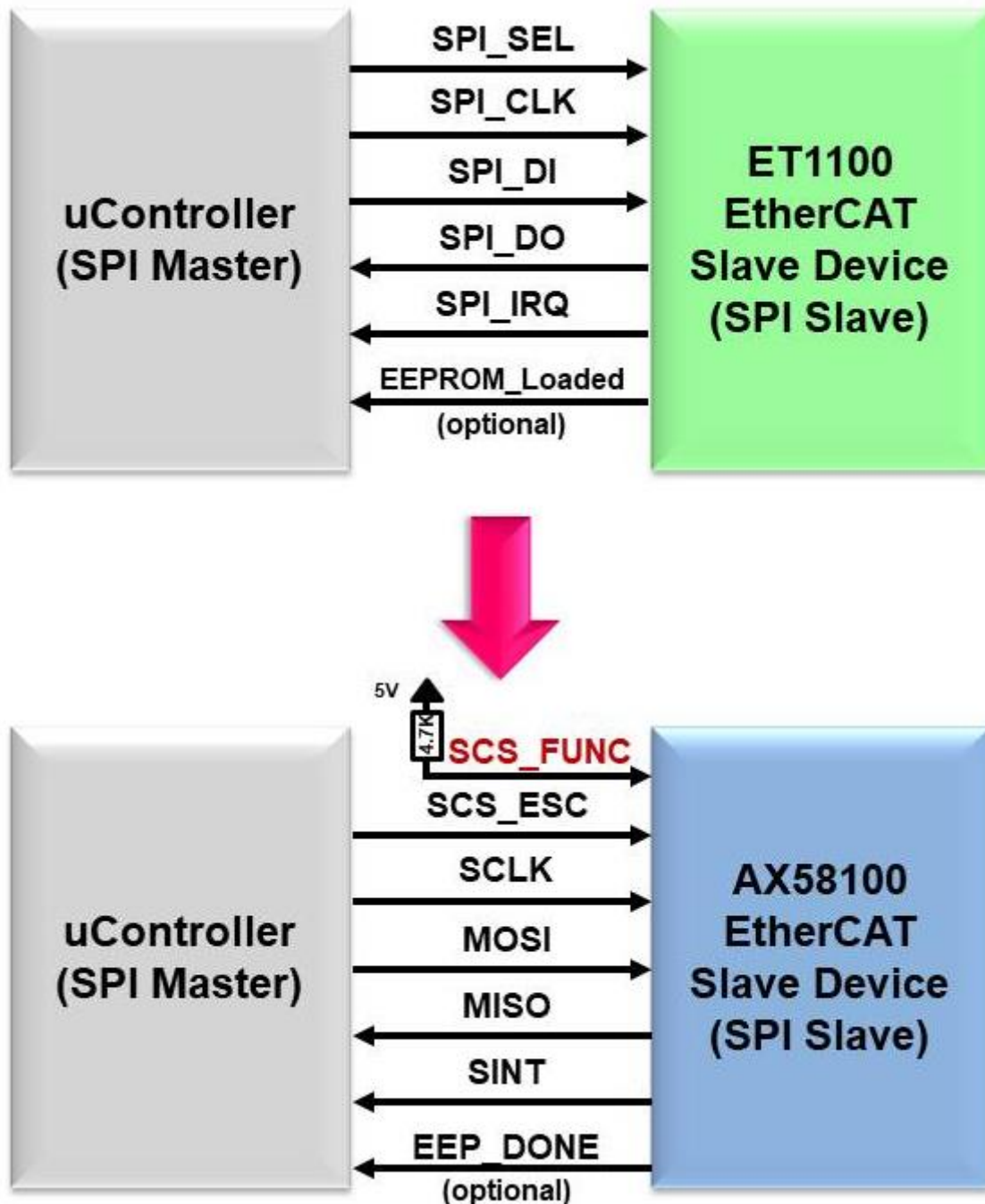


Figure 3-3. SPI Slave PDI Interface Hardware Transition

### 3-5. Local Bus PDI

The following are the hardware transition notes for Local Bus PDI applications to migrate from Beckhoff ET1100 to AX58100.

1. Pull high the LFCSn signal via a 4.7K Ohm resistor.
2. AX58100 supports 14-bit Local Bus Address bus (LA[13:0]). Keep the Address bus bit 15 & 14 of uController Local Bus interface floating directly.
3. AX58100 supports a LRDY signal to indicate the Local bus ready. The LRDY signal is an inverted polarity of ET1100 BUSY signal.
4. The EEP\_DONE signal is optional to indicate the ESC PDI bus is active.

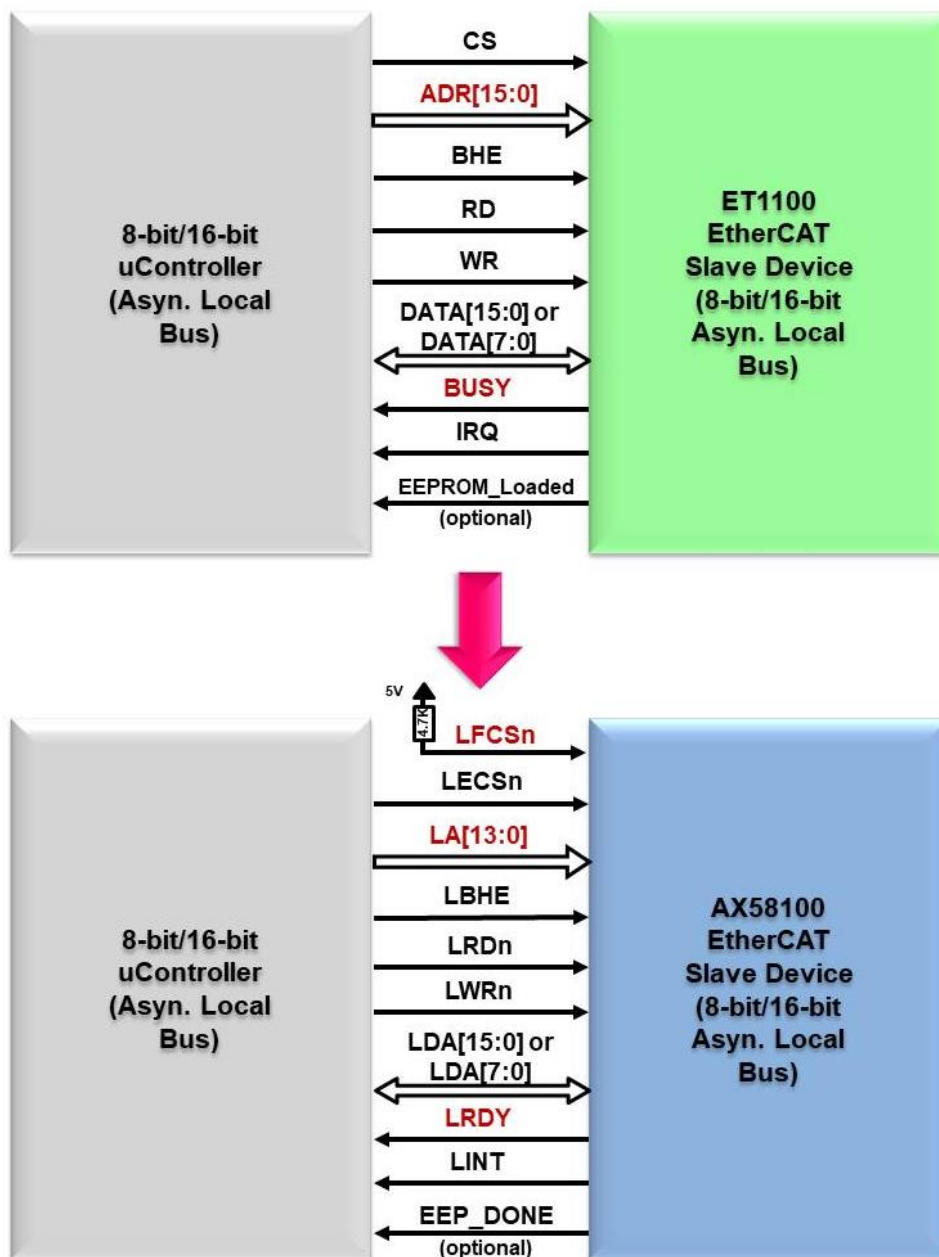


Figure 3-4. Asynchronous 8/16-bit Local Bus PDI Interface Hardware Transition

### 3-5-1. Asynchronous 8-bit Local Bus PDI

The following is a sample hardware transition for Asynchronous 8-bit Local Bus PDI applications.

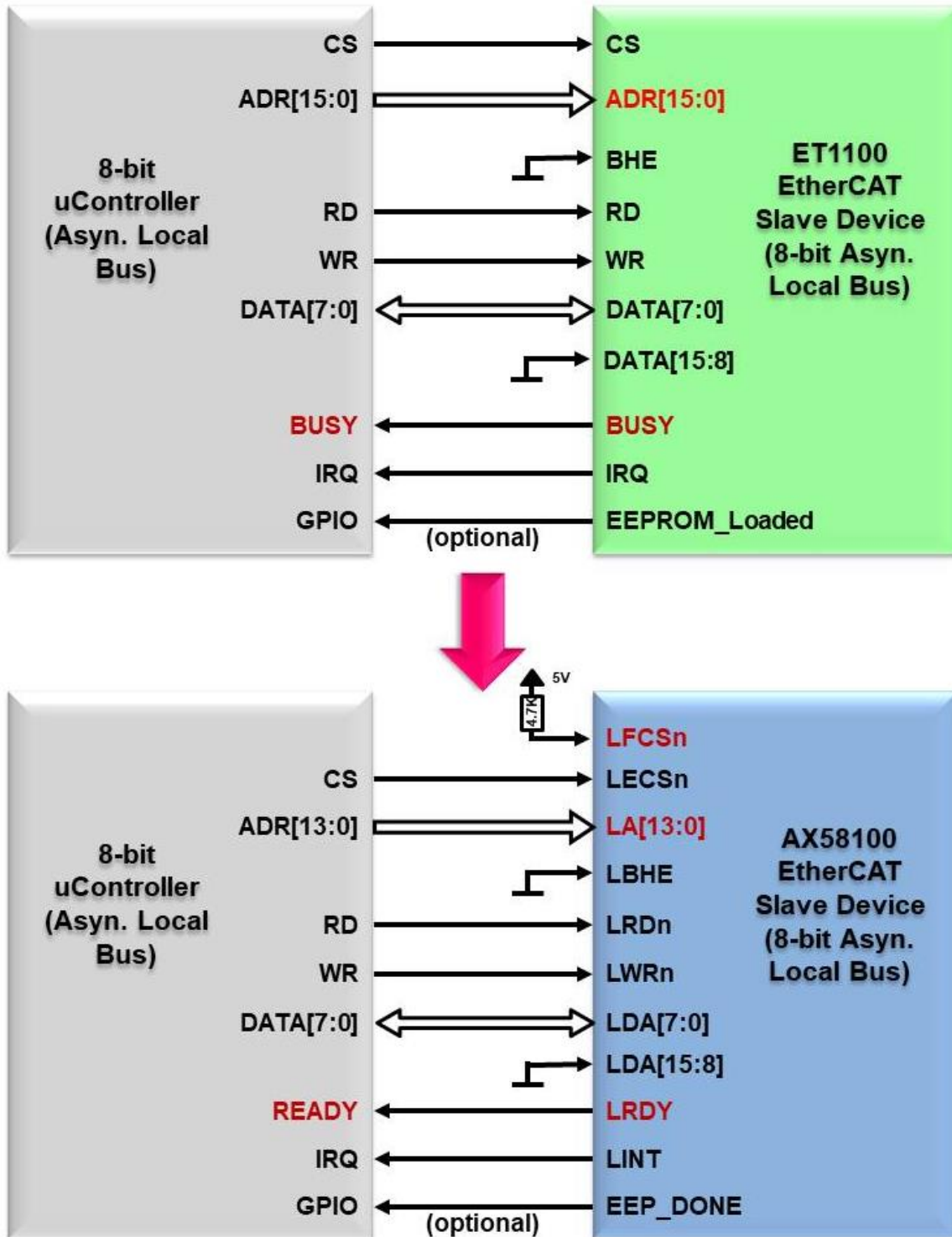


Figure 3-5. Asynchronous 8-bit Local Bus PDI Hardware Transition Example

### 3-5-2. Asynchronous 16-bit Local Bus (with 16-bit Addressing Only) PDI

The following is a sample hardware transition for Asynchronous 16-bit Local Bus (with 16-bit Addressing Only) PDI applications.

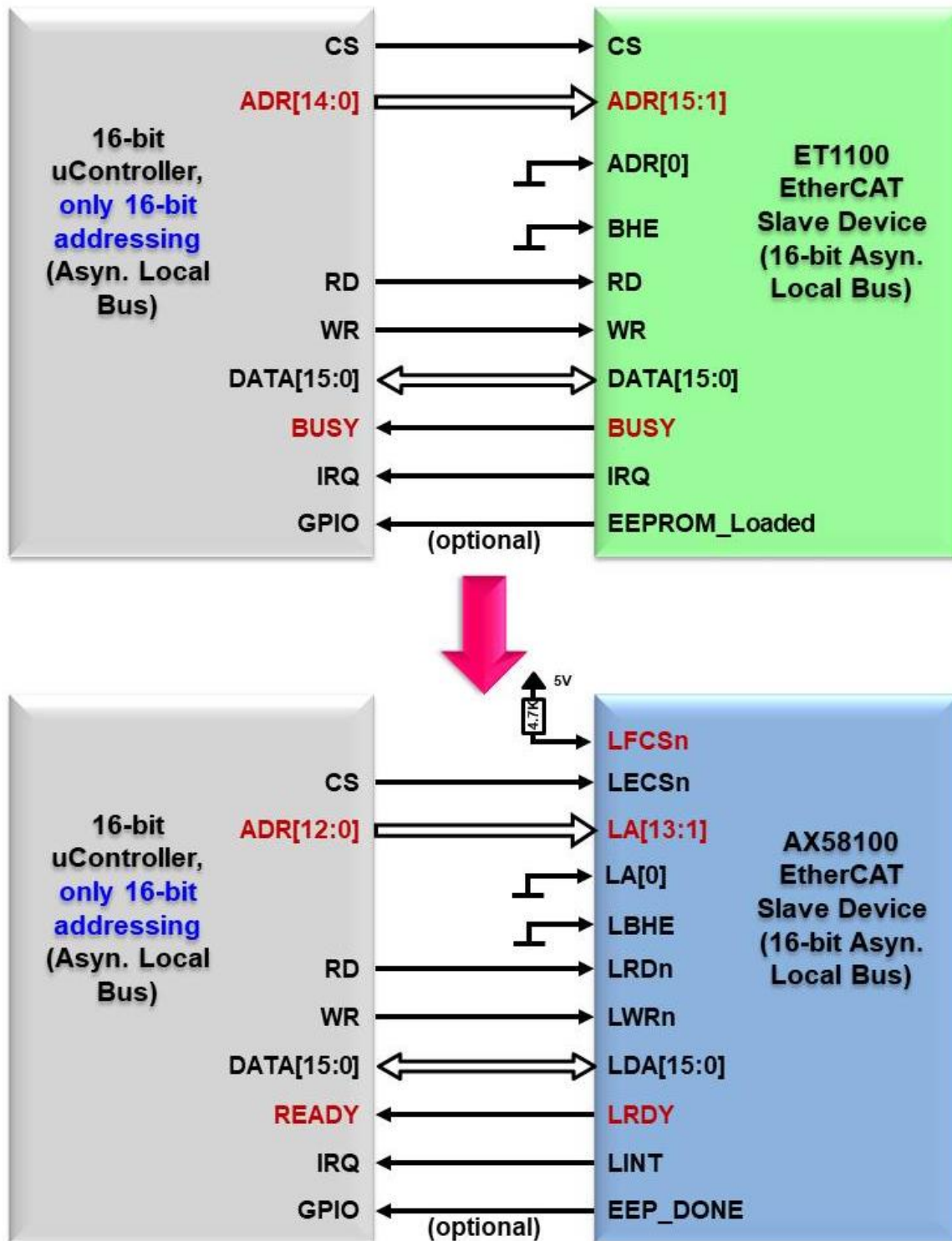


Figure 3-6. Asynchronous 16-bit Local Bus (with 16-bit Addressing Only) PDI Hardware Transition Example

## 4. Software Transition

This section indicates the software design considerations while migrating from Beckhoff ET1100 ESC solution to AX58100 ESC solution.

Basically the AX58100 ESC is licensed from Beckhoff Automation so there is no special effort to port the firmware from ET1100 ESC solution to AX58100 ESC solution except the different EtherCAT Slave Controller hardware configuration as described in below section.

### 4-1. EtherCAT Slave Information (ESI) File

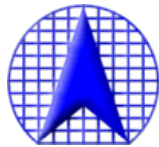
The AX58100 EtherCAT Slave Controller (ESC) configuration is different from ET1100. Please follow below procedures to change the ESC Configuration Area setting in the ESI file.

1. Open the ESI file (<FileName>.XML) to be changed in a text editor.
2. Find the “ConfigData” variable as below figure to change the ESC Configuration Area value based on your AX58100 hardware designs.

Please refer to *AX58100 ESI Design Note* and Section 3.2 “*Hardware Configuration EEPROM (HWCFGEE)*” of *AX58100 Datasheet* for details.

```
<Eeprom>  
  <ByteSize>2048</ByteSize>  
  <ConfigData>040f0044102700f0000050000001</ConfigData> ESC Configuration Area  
</Eeprom>
```

Figure 4-1. Setting the ESC Configuration Area value of ESI File



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