Features

- **Dual-CPU Architecture for Application and WLAN Protocol Processing**
  - 8-bit pipelined RISC, single cycle per instruction operating up to 80MHz and 100% software compatible with standard 8051/80390
  - Supports power management unit, programmable watchdog timer, three 16-bit timer/counters, millisecond timer and real-time clock (RTC) controller
  - Supports CPU Debugger for connecting to In-Circuit Emulation (ICE) adaptor
- **Main CPU (MCPU) for Application and TCP/IP**
  - Supports DMA Controllers (7 DMA channels) and memory arbiter for fast data movement during network protocol stack processing and peripheral communications
  - Supports TCP/IP accelerator in hardware (IP/TCP/UDP/ICMP/IGMP checksum and ARP) to improve network transfer throughput
  - Supports TCP, UDP, ICMP, IGMP, IPv4, DHCP, BOOTP, ARP, DNS, SMTP, SNTP, UPnP, PPPoE and HTTP in software
  - Supports network boot over Ethernet or Wi-Fi using BOOTP and TFTP
  - 2 external interrupt sources with 2 priority levels
- **Program and Data Memory**
  - On-chip 16KB SRAM for MCPU program code mirroring and on-chip 1MB shared Flash memory for MCPU and WCPU program code
  - Supports In-System Programming (ISP) for initial Flash memory programming via UART or ICE adaptor
  - Supports reprogrammable boot code and In-Application Programming (IAP) to update boot code or run-time firmware through Ethernet, Wi-Fi or UART interface (US Patent Approval)
  - Supports Program Loader to shadow MCPU program code to external SRAM for high performance applications
  - On-chip 64KB data memory for MCPU, expandable up to 2MB through External Memory Interface; on-chip 32KB data memory for WCPU
- **Wi-Fi CPU (WCPU) and 802.11a/b/g Compatible WLAN MAC/Baseband Processor**
  - Supports operation in Infrastructure, Simple AP or Ad-Hoc (IBSS) network topology
  - Supports DSSS and CCK: 1, 2, 5.5 & 11 Mbps
  - Supports OFDM: 6, 9, 12, 18, 24, 36, 48 & 54 Mbps
  - Supports 802.11i security

Product Brief

- Supports 802.11e QoS with 1 TX queue but selectable AC for user's application data
- Integrates on-chip RXIQ ADC, TXIQ DAC and TSSI ADC for interfacing to RF Transceiver
- Supports Ethernet to Wi-Fi packet format translation through DMA transfer between MCPU's data memory and WCPU's data memory and between WCPU's data memory and WLAN MAC
- Supports various Wi-Fi Management frames processing with hardware accelerator such as MIC, SHA-1/MD-5 transform, AES key unwrap, pseudo-random number generator (PRNG) and 32-bits arithmetic
- Supports 3 Wi-Fi power saving modes with auto-wakeup for Beacon frame reception
- Supports 1 UART for WCPU console debug, 1 external interrupt and access to I^2C interface

- **10/100M Fast Ethernet MAC**
  - IEEE 802.3 10Base-T/100Base-TX compatible Fast Ethernet MAC with dedicated 12KB SRAM for packet buffering
  - Supports full-duplex with flow control and half-duplex with backpressure
  - Supports MII, RMII, Rev-MII and Rev-RMII interfaces
  - Supports Ethernet Wake-On-LAN (WOL) by link-up, AMD Magic Packet and Microsoft Wakeup Frame
- **Peripheral Communication Interfaces**
  - 4 UART interfaces (2 supporting DMA mode, Modem control, remote wake-up and up to 921.6Kbps baud)
  - High Speed SPI interface with DMA mode (3 masters or 1 slave mode)
  - 1 I^2S or PCM interface with DMA mode
  - Local Bus host interface with DMA mode (master or slave mode)
  - 1 I^2C interface (master or slave mode)
  - 5 channels of Programmable Counter Array
  - 1 1-Wire controller interface
  - 4 GPIO ports of 8 bits each
- Integrates 32.768KHz crystal oscillator IO (with independent power input) for RTC and auto-wakeup timer of Wi-Fi power saving mode
- Integrates on-chip 80MHz PLL to operate with external 40MHz oscillator
- Integrates on-chip power-on reset circuit
- 128-pin LQFP RoHS compliant package
- Operating temperature range: 0˚C to +70˚C

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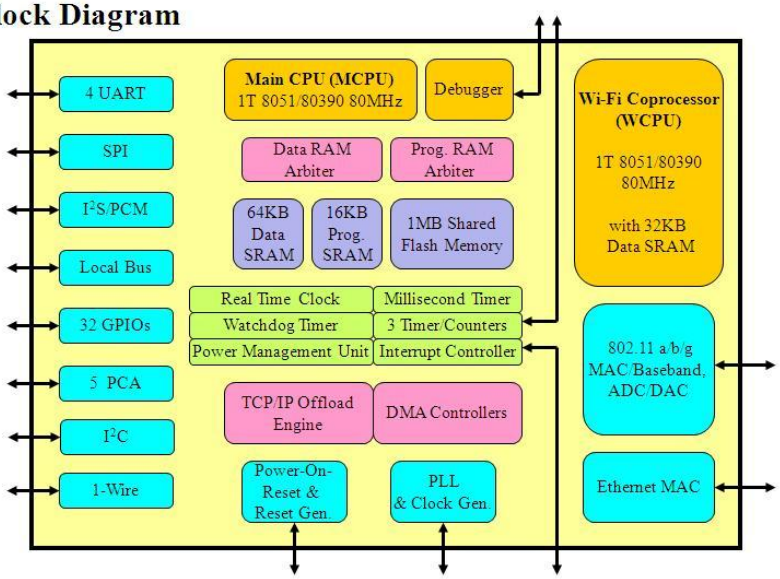
Product Description

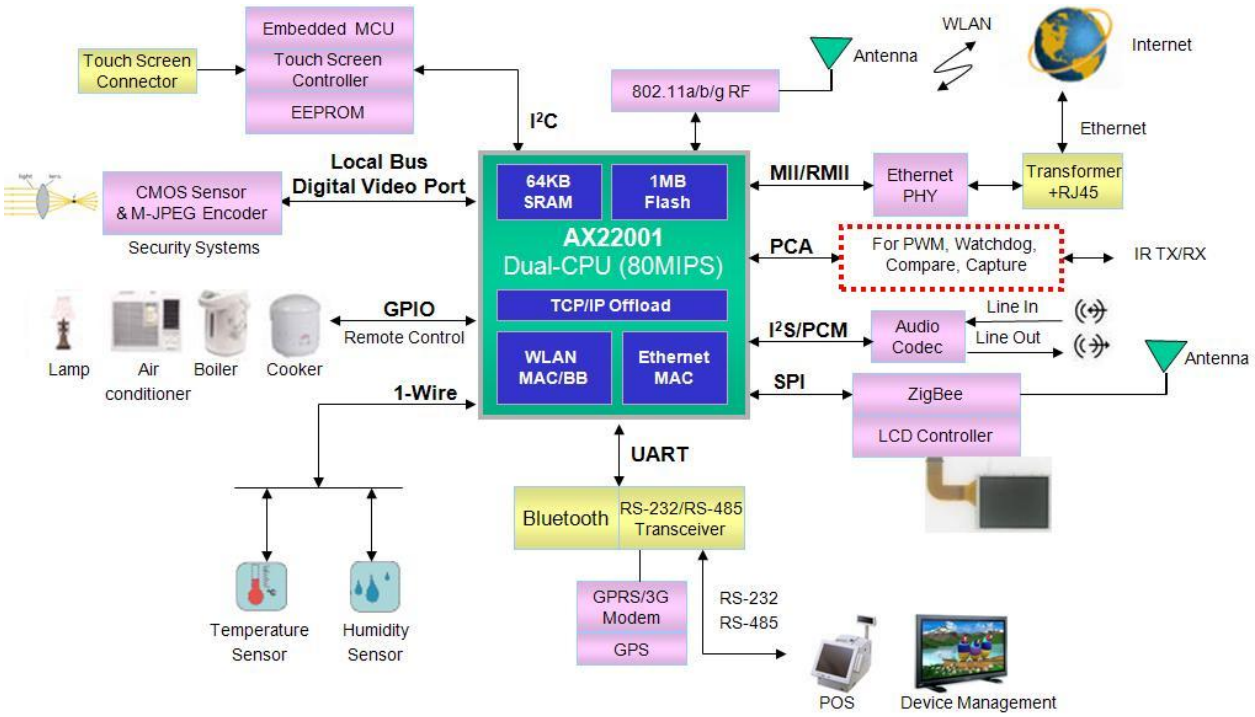
AX22001, Single Chip Micro-controller with TCP/IP and 802.11 WLAN MAC/Baseband, is a System-on-Chip (SoC) solution which offers high performance dual-CPU architecture with on-chip 1MB shared Flash as Program Memory, on-chip 64KB Data Memory for Main CPU (MCPU), on-chip 32KB Data Memory for Wi-Fi CPU (WCPU), TCP/IP accelerator, 802.11a/b/g compatible WLAN MAC/Baseband, Fast Ethernet MAC, and rich communication peripherals for wide varieties of application which need access to the wired/wireless LAN or Internet.

Block Diagram



The dual-CPU architecture of AX22001 utilizes the MCPU for applications and TCP/IP processing, and the WCPU for WLAN protocol processing and Ethernet to WLAN packet format translation. The built-in WLAN MAC and Baseband processor are compatible with IEEE 802.11a/b/g standard, and support security features compatible with 802.11i and QoS features compatible with IEEE 802.11e, and support operation in Infrastructure, Simple AP or Ad-Hoc (IBSS) network topology.

In addition to standalone application, AX22001 with TCP/IP protocol suite running on-chip and various parallel and serial host interfaces supported, such as Local Bus Interface, High Speed UART or High Speed SPI, can be used as a network co-processor to offload TCP/IP and WLAN protocol processing loading from system CPU in an embedded system.

AX22001 provides cost effective wire or wireless networking solution to enable simple, easy, and low cost Internet connection capability for many applications, such as consumer electronics, networked home appliances, industrial equipments, security systems, remote data collection equipments, remote control, remote monitoring, and remote management.

Target Applications